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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A167A/E	Rev.	1.00
Title	R8C/Tiny Series Notes on Timer RB		Information Category	Technical Notification		
Applicable Product	See Below	Lot No. --	Reference Document			

1. Usage Notes

Note 1.

In timer RB programmable waveform generation mode, if all of the following generation conditions are met, reflecting a value written into the timer RB secondary register (TRBSC register) is delayed.

Generation conditions:

(1) When the timer RB count start bit (TSTART bit) is set to 1
(2) When the timer RB prescaler (TBPRE register) is set to 00h
(3) When writing to the timer RB primary register (TRBPR register) is completed during interval A shown in Figure 1

If writing to the TRBPR register is completed during interval A (one cycle of the count source) just before the end of the second period in Figure 1, a new TRBPR register setting value is reflected during the primary period in the next cycle, but a new TRBSC register setting value is not reflected during the secondary period. A new TRBSC register setting value is reflected after a one-cycle delay.

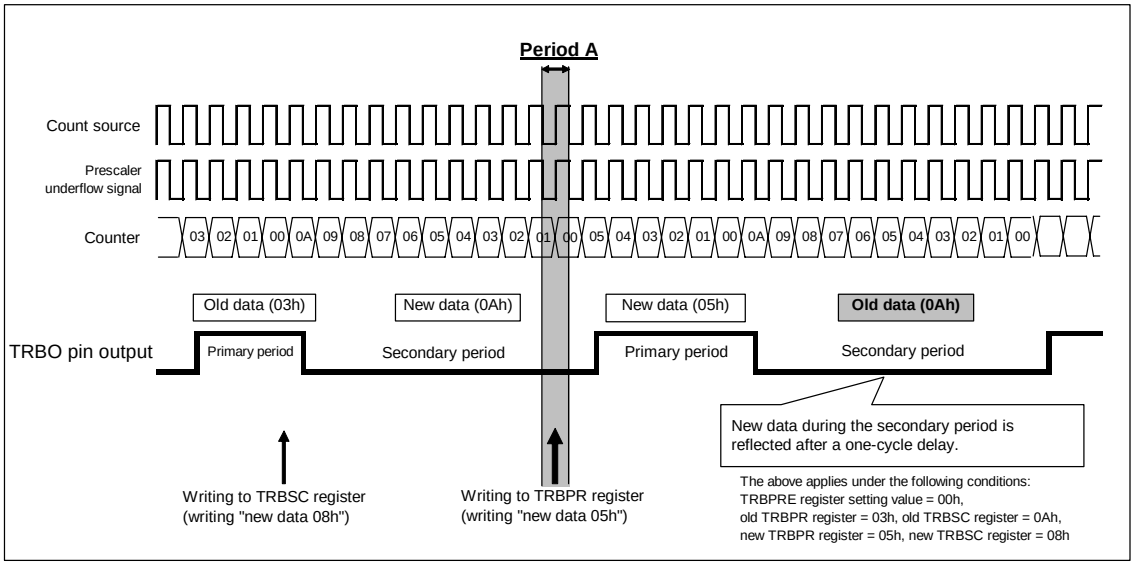

Figure 1 TRBPR Register Writing Timing When Symptom Occurs

Note 2.

In timer RB programmable wait one-shot generation mode, if all of the following generation conditions are met, reflecting a value written into the TRBSC register is delayed.

Generation conditions:

(1) When the TSTART bit is set to 1
(2) When writing to the TRBPR register is completed during interval A shown in Figure 2
(3) When a one-shot trigger (writing 1 to TOSST bit or INT0 pin one-shot trigger enabled) is generated during interval B shown in Figure 2

If writing to the TRBPR register is completed during interval A in Figure 2 and a one-shot trigger is generated during period B, a new TRBPR register setting value is reflected during the primary period, but a new TRBSC register setting value is not reflected during the secondary period. A new TRBSC register setting value is reflected at the next one-shot pulse.

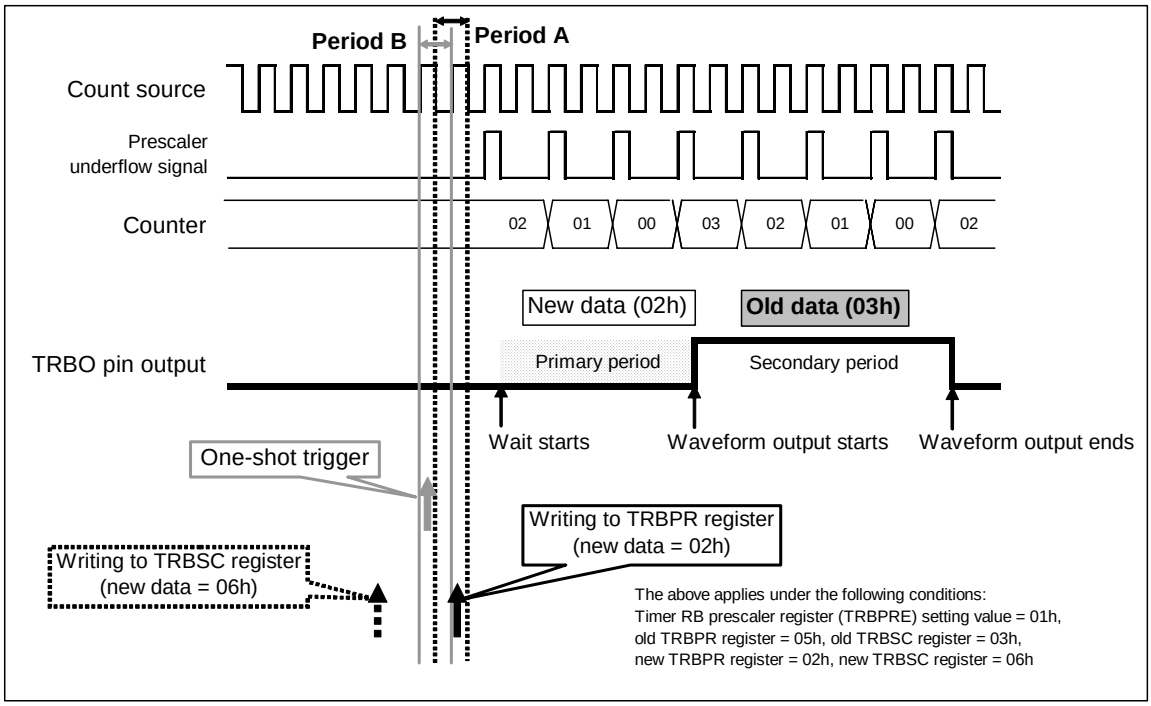

Figure 2 Programmable Wait One-Shot Generation Mode Timing When Symptom Occurs

Note 3.

In timer RB programmable one-shot generation mode and programmable wait one-shot generation mode, if all of the following generation conditions are met, no timer operation takes place and no waveform is output.

Generation conditions:

(1) The TRBPRE register is set to 00h
(2) The TRBPR register is set to 00h

Note 4.

In timer RB programmable waveform generation mode and programmable wait one-shot generation mode, if the following generation conditions occur in order from (1) to (3), a value written to the TRBSC register is subsequently reflected during the next secondary period even if writing is not performed to the TRBPR register.

Generation conditions in programmable waveform generation mode:

(1) When the TSTART bit is set to 1, registers TRBSC and TRBPR are written in order
(2) When the TSTART bit is set to 0 (including when registers TRBSC and TRBPR are updated) then this bit is set to 1 again
(3) When the TSTART bit is set to 1, the TRBSC register is written again before the end of the next secondary period

Note that the conditions are satisfied without condition (2).

Generation conditions in programmable wait one-shot generation mode:

(1) When the TSTART bit is set to 1, registers TRBSC and TRBPR are written in order
(2) When the TSTART bit is set to 0 (including when registers TRBSC and TRBPR are updated) then this bit is set to 1 again
(3) When the TSTART bit is set to 1, the TRBSC register is written again before a one-shot trigger is generated

Note that the conditions are satisfied without condition (2).

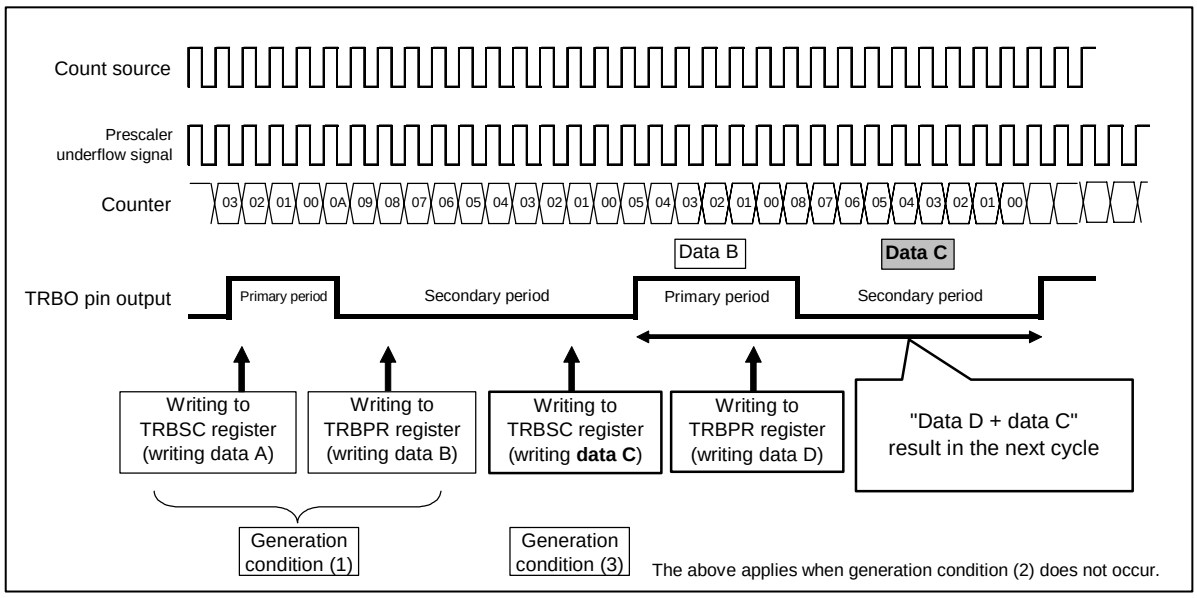

Figure 3 Timing When Symptom Occurs (Programmable Waveform Generation Mode)

Note 5.

In all timer RB modes, if writing is performed to the applicable registers below during count operation (TCSTF bit is set to 1), writing to the same register is not accepted for a certain period.
Applicable registers: TRBPRE register, TRBPR register

Generation conditions:

(1) TRBPRE register

If the TRBPRE register is written during count operation (TCSTF bit is set to 1) and when the prescaler value shown in Figure 4 is any N (period C), writing to the TRBPRE register is not accepted when the consecutive prescaler value is N-1 (period D).

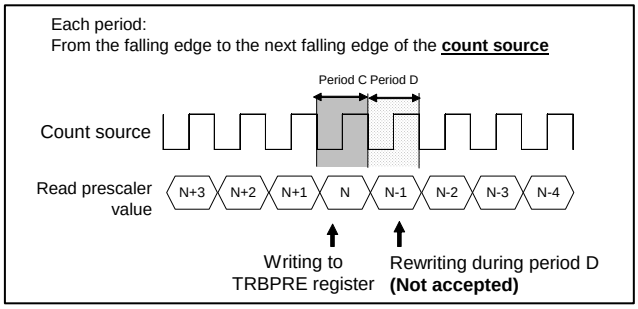

Figure 4 Continuous Writing to TRBPRE Register

(2) TRBPR register

i) In timer mode and programmable waveform generation mode

If the TRA register is written during count operation (TCSTF bit is set to 1) and when the counter value shown in Figure 5 is any N (period E), writing to the TRBPR register is not accepted when the consecutive counter value is N-1 (period F).

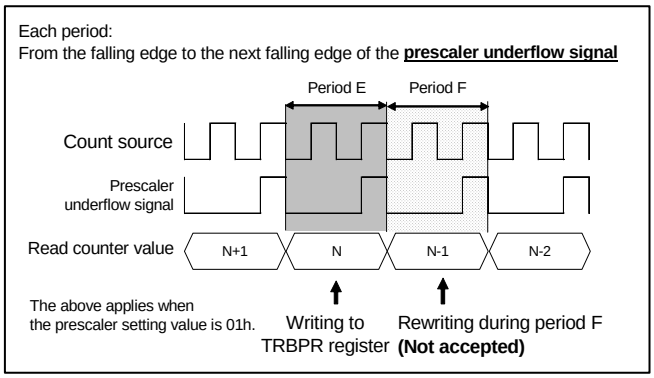

Figure 5 Continuous Writing to TRBPR Register in Timer Mode and Programmable Waveform Generation Mode

ii) In programmable one-shot generation mode and programmable wait one-shot generation mode

During count operation (TCSTF bit is set to 1) and during one-shot operation (timer RB one-shot status flag bit (TOSSTF bit) is set to 1), if the TRBPR register is written when the counter value shown in Figure 6 is any N (period G'), writing to the TRA register is not accepted when the consecutive counter value is N-1 (period H').

During count operation (TCSTF bit is set to 1) and while one-shot operation is stopped (TOSSTF bit is set to 0), if the TRBPR register is written during interval G in Figure 6, writing to the TRBPR register is not accepted during consecutive interval period H.

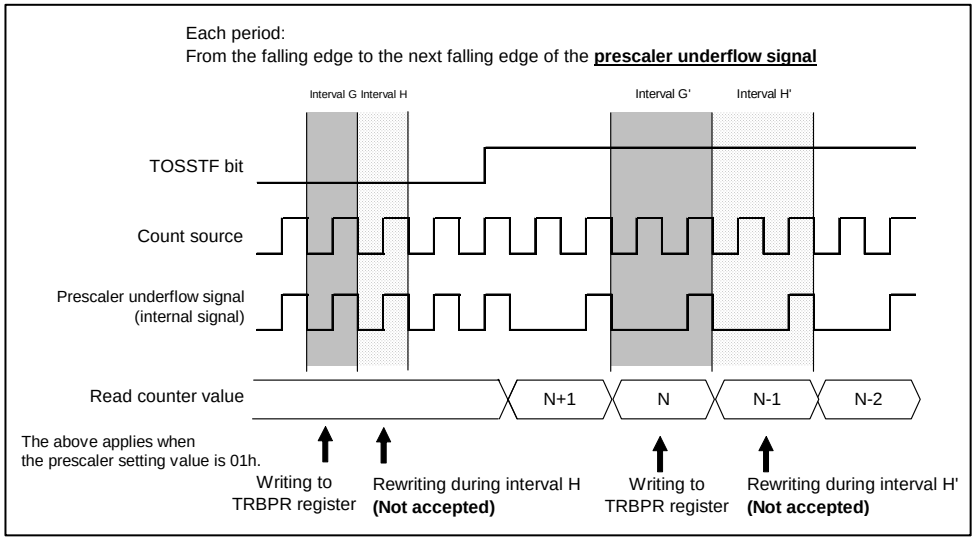

Figure 6 Continuous Writing to TRBPR Register in Programmable One-Shot Generation Mode and Programmable Wait One-shot Generation Mode

Note 6.

In timer RB programmable waveform generation mode, if all of the following conditions are met, operations from (a) to (c) will take place:

(a) A timer RB interrupt is generated.
(b) The TOCNT setting value is reflected.
(c) The TRBPR register value is reloaded into the counter.

Generation conditions:

(1) When the TSTART bit is set to 1
(2) When the TSTART bit is set to 0 (count stops) during two or three cycles of the count source before the end of the primary period

2. Countermeasures

The following shows the necessary workarounds in each mode for the six notes above.

[Timer mode] (workaround for note 5)

The following workaround should be performed in timer RB timer mode.
To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

[Timer RB programmable waveform generation mode] (workaround for notes 1, 4, 5, and 6)

The following three workarounds should be performed in timer RB programmable waveform generation mode.

1. To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

   - When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
   - When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

2. To change registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), synchronize the TRBO output cycle using a timer RB interrupt, etc. This operation should be preformed only once in the same output cycle. Also, make sure that writing to the TRBPR register does not occur during period A shown in Figures 7 and 8.

   The following shows the detailed workaround examples.

   Workaround example (1): As shown in Figure 7, write to registers TRBSC and TRBPR in the timer RB interrupt routine.

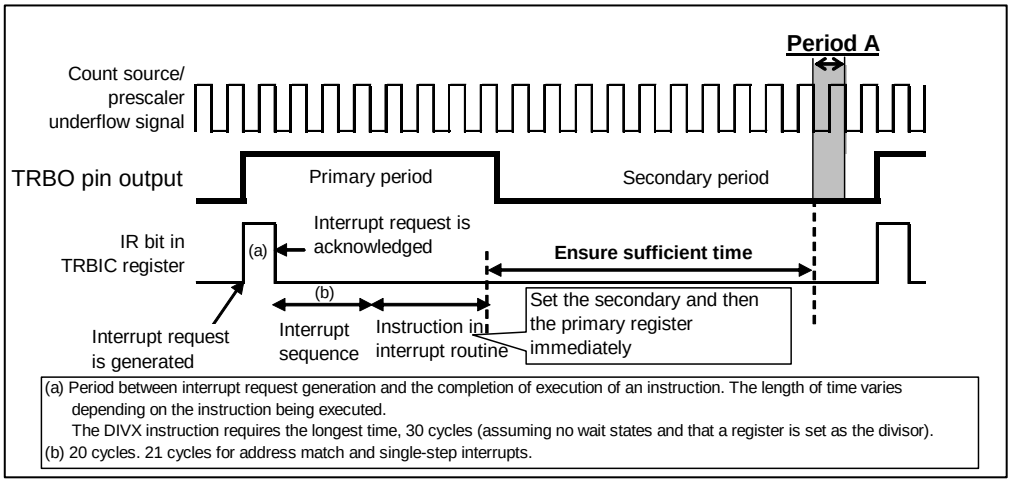

Figure 7 Workaround Example (1) When Timer RB interrupt is Used

Workaround example (2): As shown in Figure 8, detect the start of the primary period by the TRBO pin output level and write to registers TRBSC and TRBPR. If the port 1_3 bit value is read after the port 1_3 direction bit (PD1_3 bit) is set to 0 (input), the read value indicates the TRBO pin output value.

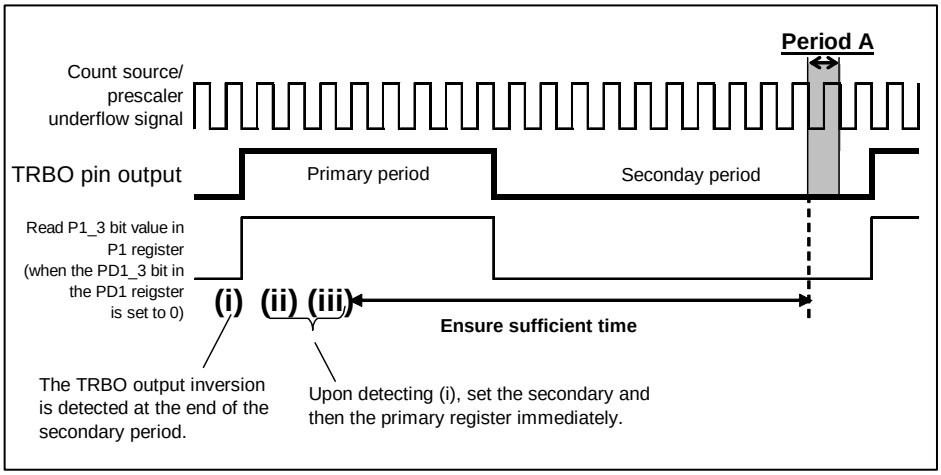

Figure 8 Workaround Example 2 When TRBO Output Value is Read

3. To stop the timer counting, use the timer RB count forcible stop bit (TSTOP bit) in the timer RB control register (TRBCR register). In this case, registers TRBPRE and TRBPR are initialized and their values are set to the values after reset.

[Timer RB programmable one-shot generation mode] (workaround for notes 3 and 5)

The following two workarounds should be performed in timer RB programmable one-shot generation mode.

1. To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

   - When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
   - When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

2. Do not set both the TRBPRE and TRBPR registers to 00h.

[Timer RB programmable wait one-shot generation mode] (workaround for notes 2, 3, 4, and 5)

The following three workarounds should be performed in timer RB programmable wait one-shot generation mode.

1. To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

   - When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
   - When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

2. Do not set both the TRBPRE and TRBPR registers to 00h.

3. Set registers TRBSC and TRBPR using the following procedure.

1) To use “INT0 pin one-shot trigger enabled” as the count start condition
The following procedures should be performed to prevent the conditions shown in Figure 2.

Workaround example 1: Once the completion of the waveform output is detected using a timer RB interrupt, etc., immediately set the TRBSC register and then the TRBPR register. (This is enabled only when a sufficient time period has been ensured before the next INT0 input after the completion of the waveform generation.)

Workaround example 2: After setting the INOSTG bit in the TRBIOC register to 0 (INT0 one-shot trigger disabled), set the TRBSC register and then the TRBPR register. After 0.5 or more cycles of the count source, set the INOSTG bit to 1 (INT0 one-shot trigger enabled). (In this case, there is a period where no INT0 input is available).

2) To use “writing 1 to TOSST bit” as the start condition
Set the TRBSC register, the TRBPR register, and TOSST bit. At this time, allow an interval of 0.5 or more cycles of the count source before writing to the TOSST bit and after writing to the TRBPR register.

3. Applicable Products

R8C/20 Group, R8C/21 Group, R8C/22 Group, R8C/23 Group,
R8C/24 Group, R8C/25 Group, R8C/26 Group, R8C/27 Group,
R8C/28 Group, R8C/29 Group, R8C/2A Group, R8C/2B Group,
R8C/2C Group, R8C/2D Group