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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A026A/E	Rev.	1.00
Title	R8C/LAxx Group Descriptions Complemented and Revised in the User's Manual: Hardware		Information Category	Technical Notification		
Applicable Products	R8C/LA3A Group R8C/LA5A Group R8C/LA6A Group R8C/LA8A Group R8C/LAPS Group	Lot No. ——	Reference Document			

Descriptions in the User's Manual: Hardware have been complemented or revised for the above applicable products.

The functions described below do not exist in some MCUs. Refer to the applicable User's Manual: Hardware for details.

1. CPU clock when exiting stop mode or power-off 2 mode

   The clock divided by 8 specified by bits CM36 and CM37 in the CM3 register is used as the CPU clock when the MCU exits stop mode or power-off 2 mode by a peripheral function interrupt. For more details, refer to the CM3 and CM0 register diagrams in the User's Manual: Hardware.

2. Pin states in stop, power-off 0, and power-off 2 modes.

   The following shows pin states in stop, power-off 0, and power-off 2 modes.

Pin	Stop Mode	Power-Off 0 Mode	Power-Off 2 Mode
I/O port	Retain the status immediately before entering stop mode	High impedance	Retain the status immediately before entering power-off 2 mode
When selecting XIN, XOUT functions (CM13 = 1)	Comply with the settings of P9_0 and P9_1	High impedance	Comply with the settings of P9_0 and P9_1
XCIN, XCOUT	Oscillation stops (high impedance)	Oscillation stops (high impedance)	Oscillate
When selecting COM, SEG, COMEXP functions	Output low	Output low	Output low
When selecting the VL3 function	Output high	High impedance	Output high
When selecting the VL2 function	High impedance	High impedance	High impedance
When selecting the VL1 function	High impedance	High impedance	High impedance

3. Note on timer RJ

   When using pulse period measurement mode, if timer RJ underflow and an active edge input in the measurement pulse causes timer RJ to reload occur simultaneously, the 8 high-order bits of the measurement value retained in the read-out buffer become invalid.

4. Incorrect descriptions in the R8C/LA3A Group, R8C/LA5A Group User's Manual: Hardware, Rev.1.00 (R01UH0024EJ0100)

The program example to enter power-off 0 mode in section 10.9.4 Power-Off 0 Mode has been revised as shown below.

- Program example to enter power-off 0 mode

```
BCLR    1, FMR0          ; CPU rewrite mode disabled
MOV.B   #02H, POMCR0     ; Select power-off 0, WUKP1 input enabled
MOV.B   #88H, POMCR0     ; Fixed value
MOV.B   #15H, POMCR0     ; Fixed value
MOV.B   #92H, POMCR0     ; Fixed value
MOV.B   #25H, POMCR0     ; Fixed value
NOP
NOP
NOP
NOP                      ; Enter power-off 0 mode
BSET    1, PRCR          ; Software reset
BSET    3, PM0
```

5. Incorrect descriptions in the R8C/LAPS Group User's Manual: Hardware, Rev.1.00 (R01UH0168EJ0100)

The XIN clock input oscillation frequency, system clock frequency, and CPU clock frequency listed in Table 25.2 Recommended Operating Conditions in section 25.2 Recommended Operating Conditions have been revised as shown below.

Table 25.2 Recommended Operating Conditions

(V_{CC} = 1.8 to 5.5 V and Topr = - 20 to 85°C (N version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	XIN clock input oscillation frequency	2.7 V ≤ V_{CC} ≤ 5.5 V	2	—	20	MHz
		2.0 V ≤ V_{CC} < 2.7 V	2	—	10	MHz
		1.8 V ≤ V_{CC} < 2.0 V	2	—	8	MHz
—	System clock frequency	2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
		2.0 V ≤ V_{CC} < 2.7 V	—	—	10	MHz
		1.8 V ≤ V_{CC} < 2.0 V	—	—	8	MHz
$f_{(BCLK)}$	CPU clock frequency	2.7 V ≤ V_{CC} ≤ 5.5 V	0	—	20	MHz
		2.0 V ≤ V_{CC} < 2.7 V	0	—	10	MHz
		1.8 V ≤ V_{CC} < 2.0 V	0	—	8	MHz