1. Correction on timer RE reset bit (TRERST bit)

The follow correction to the timer RE reset bit (TRERST bit) is taken from the R8C/L35M, R8C/L36M, R8C/L38M, and R8C/L3AM Group User’s Manual: Hardware (R01UH0110EJ0100). Refer to the User’s Manual: Hardware of your product.

When setting this bit to 1, the following will occur and timer RE control circuit will be initialized. After setting this bit to 1, make sure to set it to 0.
2. Correction on notes on timer RE

The following correction to notes on timer RE is taken from the R8C/L35M, R8C/L36M, R8C/L38M, and R8C/L3AM Group User’s Manual: Hardware (R01UH0110EJ0100). Refer to the manual of your product.

22.4 Notes on Timer RE

22.4.1 Reset

A reset input does not reset the timer RE data registers that store data of seconds, minutes, hours, and days of the week. This requires the initial setting of all registers after power on.

The registers and bits associated with timer RE below will not be reset by hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, or software reset. As the content of such registers and bits are undefined after power on, initialize these registers and bits after setting the TRERST bit to 0. When the TRERST bit is set to 1, the registers and bits are set to 0, and the timer RE control circuit will be initialized. After setting the TRERST bit to 1, make sure to set it to 0.

Applicable registers and bits:
- Registers TRESEC, TREMIN, TREHR, TREWKR, and TREC2R
- Bits TCSTF, INT, TRERST, PM, H12_H24, TSTART in the TREC1 register
3. Supplement information for the setting example in output compare mode

- **TSTART in TRECR1 = 0**
  - Stop timer RE operation
- **TCSTF in TRECR1 = 0?**
  - **TOENA in TRECR1 = 0**
    - Disable the timer RE clock output
  - **TREIC ← 00h**
    - Disable timer RE interrupt
- **TRERST in TRECR1 = 1**
  - Reset the registers and bits associated with timer RE and the timer RE control circuit
- **TRERST in TRECR1 = 0**
  - **TRECSR ← 0XXX0XXXb**
    - Set in output compare mode
    - Select the count source
    - Select the clock output
  - **Set TREMIN**
    - Set the compare data
  - **TRECR2 ← X0000000b**
    - Enable or disable the compare match interrupt
    - (X = 0 or 1)
  - **Set TREIC**
    - Select the interrupt priority level
  - **TOENA in TRECR1 = 1**
    - Enable the timer RE clock output (when necessary)
  - **TSTART in TRECR1 = 1**
    - Start timer RE operation
- **TCSTF in TRECR1 = 1?**