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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A028A/E	Rev.	1.00
Title	R8C/3MQ Group Specification Change		Information Category	Technical Notification		
Applicable Product	R8C/3MQ Group R5F213MCQNNP, R5F213MAQNNP, R5F213M8QNNP, R5F213M7QNNP, R5F213M6QNNP	Lot No. NA	Reference Document	NA		

1 Introduction

This document provides the information regarding a specification change for the Datasheet and User's Manual.

1.1 Summary

1.1.1 To change the program ROM size for R5F213MCQNNP.

1.1.2 To add a usage note about the data flash for all R8C/3MQ group devices.

1.1.3 To add the detection level to the "voltage detection 0" circuit for all R8C/3MQ group devices.

1.1.4 To change the supply voltage condition of the "CPU clock frequency" specification for all R8C/3MQ group devices.

1.2 Related documents

1.2.1	R8C/3MQ Group Datasheet	Rev.1.00	R01DS0044EJ0100
1.2.2	R8C/3MQ Group User's Manual: Hardware	Rev.1.00	R01UH0117EJ0100

2 Description

2.1 To change the program ROM size for R5F213MCQNNP

The program ROM size of R5F213MCQNNP changes from 128 Kbytes to 112 Kbytes. Upper limit of the program ROM address described on the related documents changes from 23FFFh to 1FFFFh for R5F213MCQNNP. That means the program ROM block 8 address starts from 1C000h end on 1FFFFh. Also the program ROM size of block 8 changes from 32 Kbytes to 16 Kbytes. Additionally refer to the usage note about the development tool shown below in Section 3.

2.2 To add the usage note about the data flash for all R8C/3MQ group devices.

Do not execute a program on the data flash. That is to say, do not assign a program code on the data flash area.

2.3 To add the detection level to the "voltage detection 0" circuit for all R8C/3MQ group devices.

Two detection levels named "Vdet0_1" and "Vdet0_2" are added for the "voltage detection 0" circuit as figure 2.3.1. Furthermore two control bits named "VDSEL0" and "VDSEL1" for selecting the detection levels are added at OFS register as figure 2.3.2.

Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (4)		1.80	1.90	2.05	V
Additional specification	Voltage detection level Vdet0_1 (4)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (4)		2.70	2.85	3.05	V
—	Voltage detection 0 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet0_0 – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 3.0 V	—	1.5	—	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	μs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
4. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

Figure 2.3.1 Voltage Detection 0 Circuit Electrical Characteristics

Option Function Select Register (OFS)

Address 0FFFFh — Additional function

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4	R/W
b5	VDSEL1	Additional function	0 0: Do not set. 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   Initial value of OFS register is FFh. The value of OFS register changes as programmed by user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

Figure 2.3.2 Option Function Select Register (OFS)

2.4 To change the supply voltage condition of the CPU clock frequency specification for all R8C/3MQ group devices.

Minimum supply voltage when the CPU clock frequency f(BCLK) is less or equal to 8 MHz improves from 2.2 V to 2.15 V.

3 Usage note for the development tool for R5F213MCQNNP

C/C++ Compiler Package for M16C Series and R8C Family [M3T-NC30WA] and On-chip Debugging Emulators E8a, E1 and E20 do not have the choice for 112 Kbytes program ROM. The recommended changes while using these development tools are described below.

3.1 C/C++ Compiler Package for M16C Series and R8C Family [M3T-NC30WA]

In creating the new project, select “128K” for “ROM size” menu. In selecting “C source startup Application”, select “None” for “Use OnChip Debugging Emulator” menu. Address assignment of the firmware or the debug monitor for the on-chip debugging emulator is controlled by the emulator setting.

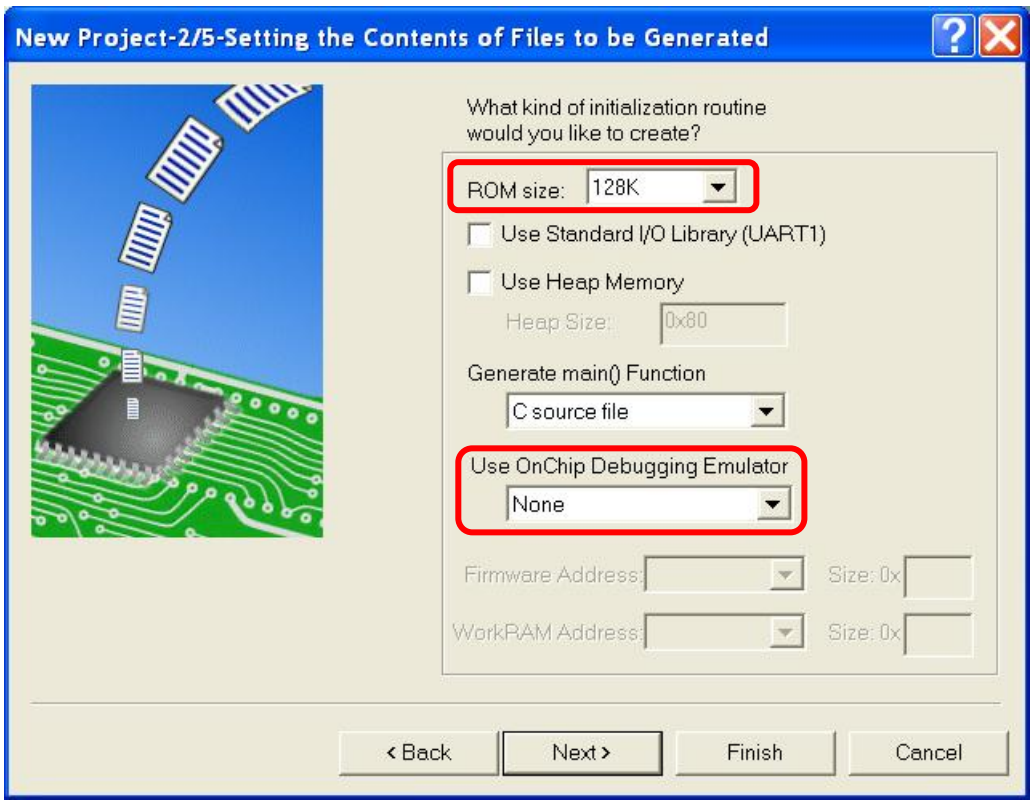

Figure 3.1 Setting of new project creation wizard 2 of 5

3.2 On-chip Debugging Emulator E8a

3.2.1 Firmware location

In starting the E8a emulator connection, select the “Firmware Location” tab on the “Emulator Setting” dialogue and check “Enable advanced setting”. Then you can select the firmware location. Select “User Flash Area” for firmware location. Specify the address among the range from 04000h to 1FFFFh and do not include the fixed interrupt vector area. For example set there as 1F800 – 1FFFF like figure 3.2.2. Do not select “Data Flash Area” for “Firmware Location” menu as the program code cannot be assigned on data flash.

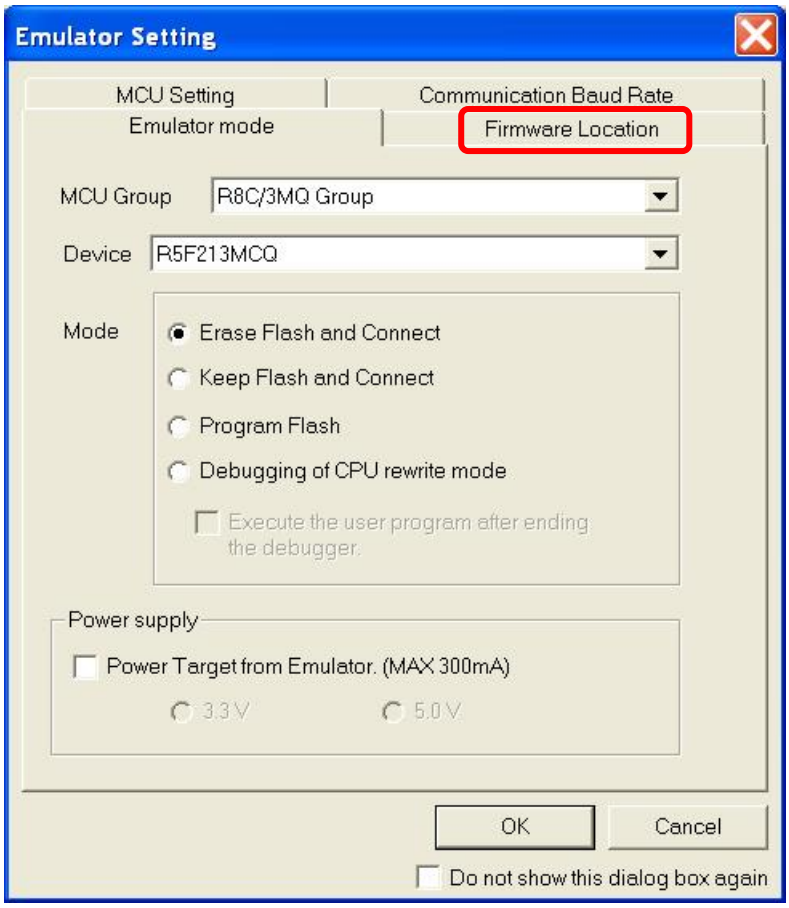

Figure 3.2.1 First “Emulator setting” dialogue for E8a

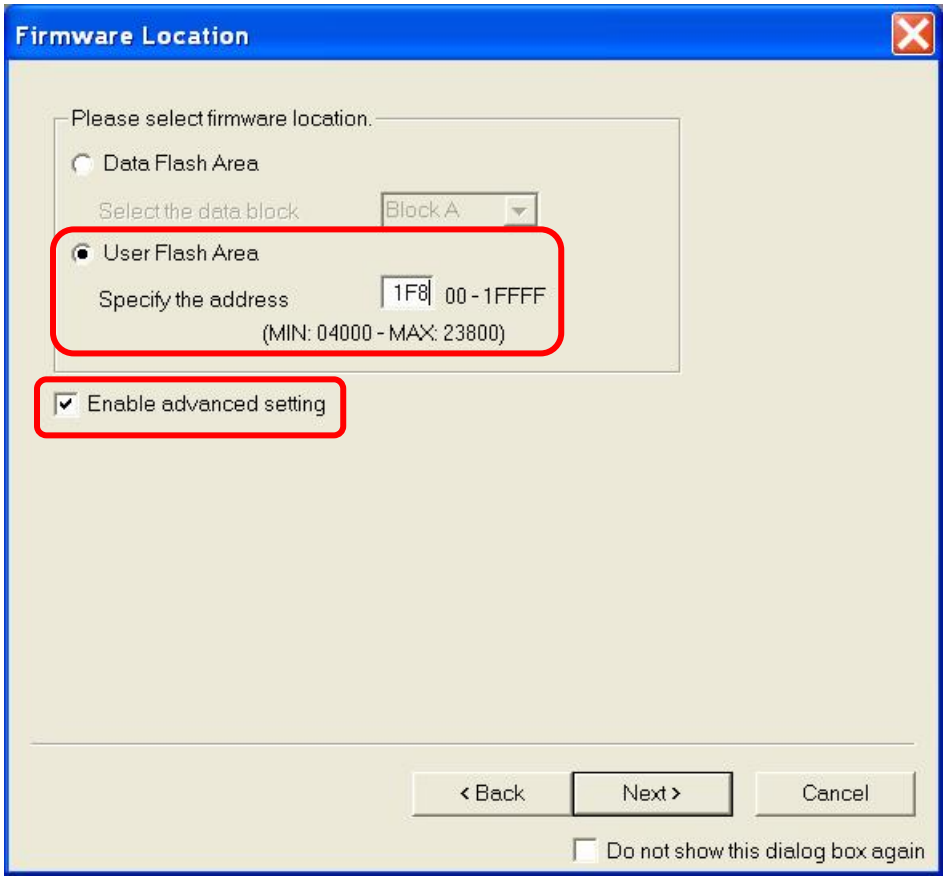

Figure 3.2.2 Second “Emulator setting” dialogue for E8a

3.2.2 Download the user program

No warning message will be displayed on the development tool window if the user program size exceeds the 112 Kbytes memory location area, in downloading the program code from the development tool to the device. Check the “map” file for the allocation of program code before download.

3.3 On-chip Debugging Emulators E1 and E20

3.3.1 Debug monitor location

In starting the E1 or E20 emulator connection, select the “System” tab on the “Configuration Properties” dialogue and specify the debug monitor location. Select “User flash area” for “Debug monitor location” menu. Specify the address among the range from 04000h to 1F800h and do not include the fixed interrupt vector area. For example set there as 1F800 – 1FFFF like figure 3.3. Do not select “Data flash area” for “Debug monitor location” menu as the program code cannot be assigned on data flash.

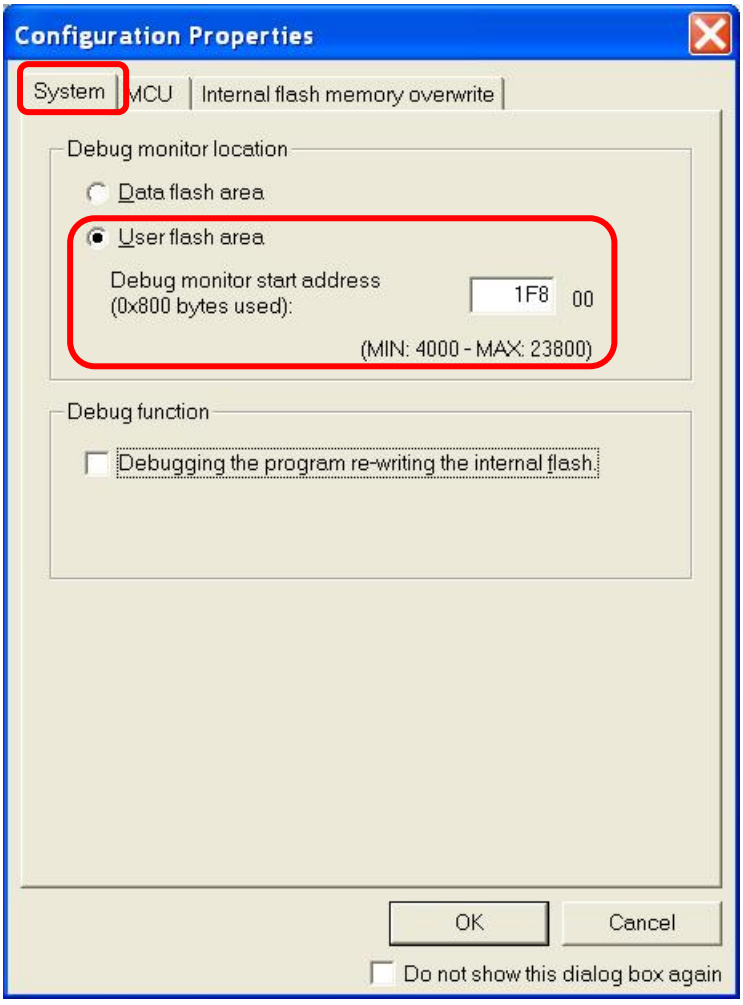

Figure 3.3 Setting of “Configuration Properties” for E1 and E20

3.3.2 Download the user program

No warning message displayed on development tool window if the user program size exceeds the 112 Kbytes memory location area, in download the program code from the development tool to the device. check the “map” file for the allocation of program code before download.

4 Future plans

A revised User’s Manual and Datasheet will be released soon as Rev. 2.00 incorporating the changes outlined in this document.