

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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# RENESAS TECHNICAL UPDATE

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RenesasTechnology Corp.

Product Category	MPU&MCU	Document No.	TN-16C-A146A/E	Rev.	1.00
Title	R8C/16, 17 Groups Precautions on Using I <sup>2</sup> C bus Interface	Information Category	Technical Notification		
Applicable Product	R8C/16, 17 Groups	Lot No.	Reference Document		
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As for the I<sup>2</sup>C bus interface included in the above applicable products, there are precautions on using it.

[Precautions on Using]

- (1) Generate the stop condition and start condition (only when retransmitting) after the 9th clock falling edge is recognized.  
Checking SCL0 bit in the I2C control register 2 (ICCR2) can recognize the 9th clock falling edge.  
When generating the stop condition and start condition (only when retransmitting) at the specific timing under the following (i) or (ii), such conditions may not be output properly. This does not occur in other cases.
  - (i) When the SCL rising edge falls behind the time specified in the section "15.6 Bit Synchronous Circuit" of the hardware manual, by the load of the SCL bus (load capacitance or pull-up resistance).
  - (ii) When the bit synchronous circuit is activated by driving SCL "L" after the falling edge of the 8th clock with the slave device.
- (2) There is the following precaution when using WAIT bit in I<sup>2</sup>C bus mode register (ICMR) with "1".  
When setting the WAIT bit to "1", and SCL is driven "L" for 2 or more transfer clocks by the slave device after the falling edge of the 8th clock, the "H" period of the 9th clock may be shortened. This does not occur in other cases.