To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Date: Mar. 26, 2010

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A011A/E	Rev.	1.00
Title	R8C Family Notes on I²C-bus Interface		Information Category	Technical Notification		
Applicable Products	See below	Lot No. —	Reference Document			

This document describes notes when using the I²C-bus interface in I²C-bus interface mode for the products shown below.

1 Applicable products

R8C/16 Group, R8C/17 Group, R8C/1A Group, R8C/1B Group
R8C/20 Group, R8C/21 Group, R8C/22 Group, R8C/23 Group, R8C/24 Group, R8C/25 Group
R8C/26 Group, R8C/27 Group, R8C/28 Group, R8C/29 Group,
R8C/2A Group, R8C/2B Group, R8C/2C Group, R8C/2D Group,
R8C/32A Group, R8C/32C Group, R8C/33A Group, R8C/33C Group, R8C/34C Group
R8C/35A Group, R8C/35C Group, R8C/36A Group, R8C/36C Group,
R8C/38A Group, R8C/38C Group, R8C/3GA Group, R8C/3JA Group,
R8C/L3AA Group, R8C/L3AB Group, R8C/L3AC Group,
R8C/L38A Group, R8C/L38B Group, R8C/L38C Group,
R8C/L36A Group, R8C/L36B Group, R8C/L36C Group,
R8C/L35A Group, R8C/L35B Group, R8C/L35C Group

2 Note on master receive mode

2.1 Note

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

2.2 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.

Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

3 Note regarding the ICE bit in the ICCR1 register and the IICRST bit in the ICCR2 register

3.1 Note

When writing 0 to the ICE bit or 1 to the IICRST bit during an I^2C-bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

3.2 Conditions when bits become undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

3.3 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

3.4 Additional descriptions regarding the IICRST bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I^2C-bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I^2C-bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.