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R7F0C003, R7F0C004, R7F0C019
Precaution of using High accuracy 1 Hz output

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Applicable Product

R7F0C003M2DFB-C
R7F0C004M2DFB-C
R7F0C019L2DFB-C

Reference Document

R7F0C003M2DFB,R7F0C004M2DFB
: R01UH0393EJ0200(Mar, 2014)
: R01UH0393CJ0200(Jan, 2015)

R7F0C019L2DFB
: R01UH0465EJ0200(Mar, 2014)
: R01UH0465CJ0200(Mar, 2015)

Precaution described below is added to the following products in the User's Manual.

List of corrections to be added in this notification

R7F0C003M2DFB, R7F0C004M2DFB: R01UH0393EJ0200

Item	Correction Item	Applicable Page	Contents
1-1	7.4.7 Clock error correction register setting procedure	P.340	Precaution added
1-2	Figure 7-1. Real-time Clock 2 Diagram	P.311	Incorrect descriptions revised

R7F0C003M2DFB, R7F0C004M2DFB: R01UH0393CJ0200

Item	Correction Item	Applicable Page	Contents
1-1	7.4.7 时钟误差校正寄存器的设定步骤	P.315	Precaution added
1-2	图7-1 高精度实时时钟的框图	P.289	Incorrect descriptions revised

R7F0C019L2DFB: R01UH0465EJ0200

Item	Correction Item	Applicable Page	Contents
1-1	7.4.7 Clock error correction register setting procedure	P.325	Precaution added
1-2	Figure 7-1. Real-time Clock 2 Diagram	P.297	Incorrect descriptions revised

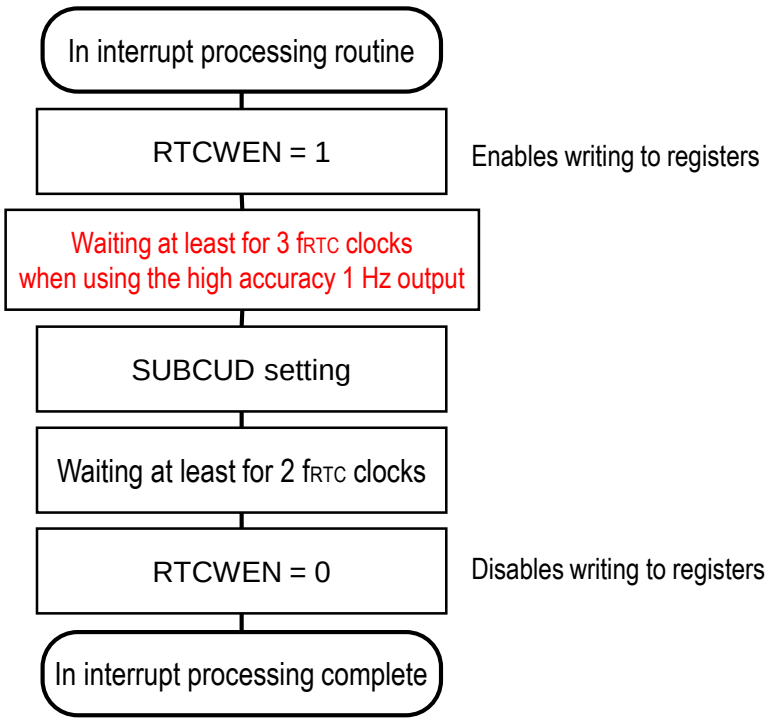
R7F0C019L2DFB: R01UH0465CJ0200

Item	Correction Item	Applicable Page	Contents
1-1	7.4.7 时钟误差校正寄存器的设定步骤	P.299	Precaution added
1-2	图7-1 高精度实时时钟的框图	P.273	Incorrect descriptions revised

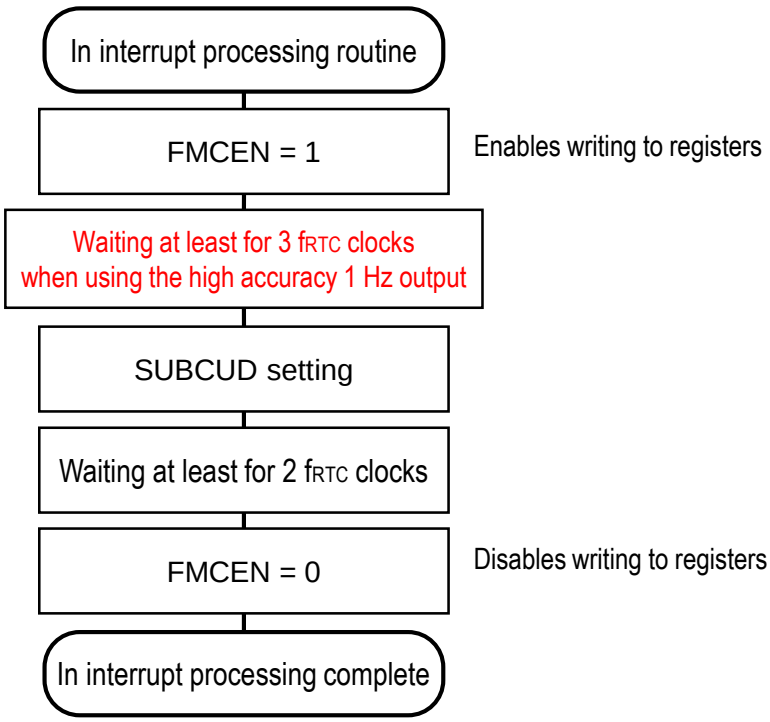
1-1. Precaution regarding the clock error correction register (SUBCUD) setting procedure when using the high accuracy 1 Hz output.

Use either of the following procedures to set the clock error correction register (SUBCUD).
In order to prevent write error to the clock register, write privilege with (2) FMCEN is recommended for rewrite of the SUBCUD register.
RTC correction may not be successful if there is a conflict between the SUBCUD register rewrite and correction timing. In order to prevent conflict between the correction timing and rewrite of the SUBCUD register, be sure to complete rewrite of the SUBCUD register before the next correction timing occurs (within approx. 0.5 seconds), which is calculated starting from the correction timing interrupt (INTRTIT) or periodic interrupt (INTRTC) that is synchronized with the correction timing.
When using the high accuracy 1 Hz output and rewriting the SUBCUD register, rewrite the SUBCUD register after waiting at least for 3 f_{RTC} clocks.

(1) Set the clock error correction register (SUBCUD) after setting RTCWEN to 1 first. Then set RTCWEN to 0 after completion of the register setting.



(2) Set the clock error correction register (SUBCUD) after setting FMCEN to 1 first. Then set FMCEN to 0 after completion of the register setting.



1-2. Root correction of the INTRTIT in the Real-time Clock 2 Diagram

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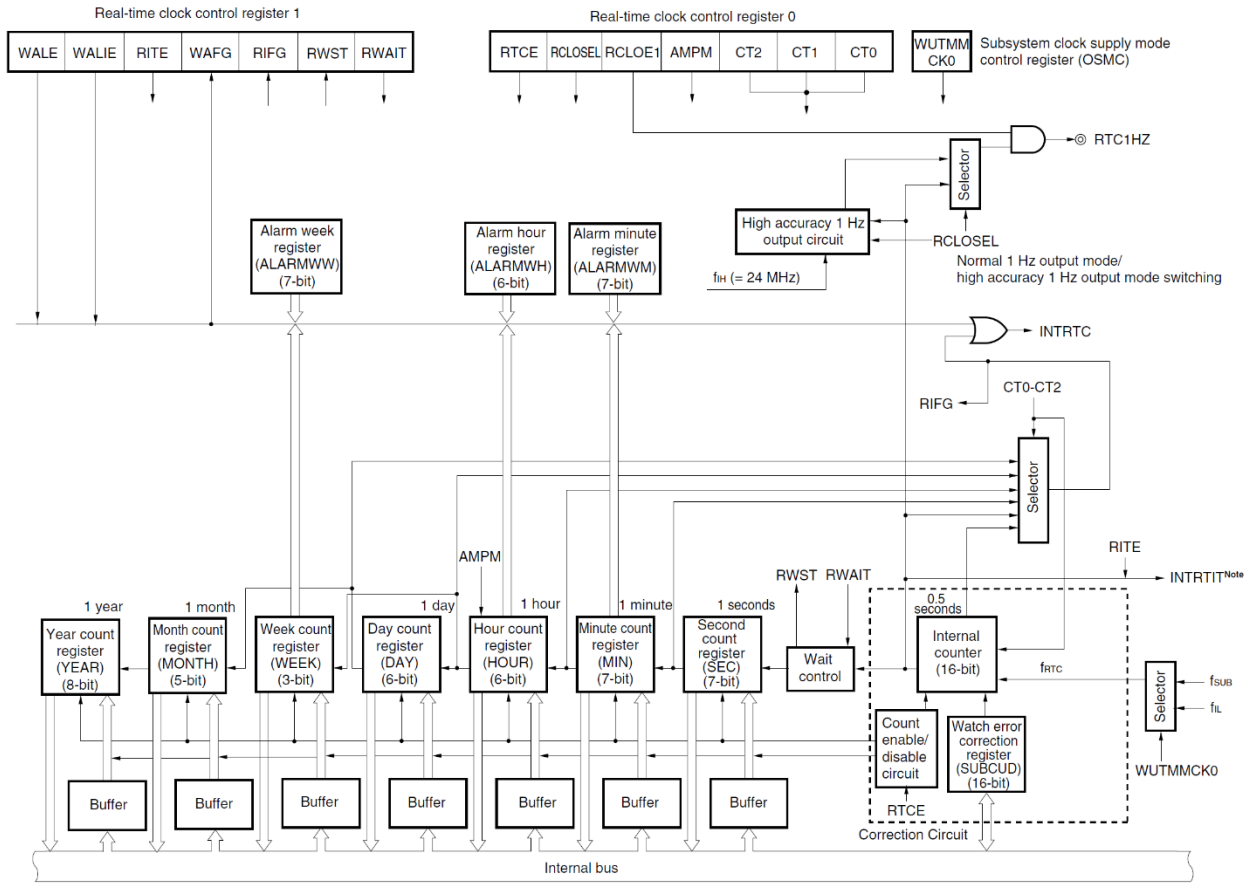
Figure 7-1. Real-time Clock 2 Diagram



Note An interrupt that indicates the timing to get the correction value from the clock error correction register (SUBCUD). The fetch timing is 1 second (f_{SUB} base) interval.