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RENESAS TECHNICAL UPDATE

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Product Category	System LSI		Document No.	TN-RZ*-A0067A/E	Rev.	1.00
Title	QSPI contoller issue		Information Category	Technical Notification		
Applicable Product	RZ/N1 Series (See below for details)	Lot No. All lots	Reference Document	RZ/N1 Series User's Manual (See below for details)		

We would like to inform about QSPI controller issue.

1. Applicable Product

Product Group	Part Number	Package Type	Configuration
RZ/N1D	R9A06G032NGBG	400BGA	Dual Cortex-A7, PRP/HSR
	R9A06G032VGBG	400BGA	Dual Cortex-A7
	R9A06G032PGBG	400BGA	Dual Cortex-A7, PRP/HSR, Security
	R9A06G032EGBG	400BGA	Dual Cortex-A7, Security
	R9A06G032VGBA	324BGA	Dual Cortex-A7
	R9A06G032EGBA	324BGA	Dual Cortex-A7, Security
RZ/N1S	R9A06G033NGBG	324BGA	Single Cortex-A7, PRP
	R9A06G033PGBG	324BGA	Single Cortex-A7, PRP, Security
	R9A06G033VGBA	196BGA	Single Cortex-A7
	R9A06G033EGBA	196BGA	Single Cortex-A7, Security
RZ/N1L	R9A06G034VGBA	196BGA	Cortex-M3

2. Reference Document

Reference document name	Document Number	Current Revision	Revised Revision
RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User's Manual: System Control and Peripheral	R01UH0751EJ****	V1.00	V1.10

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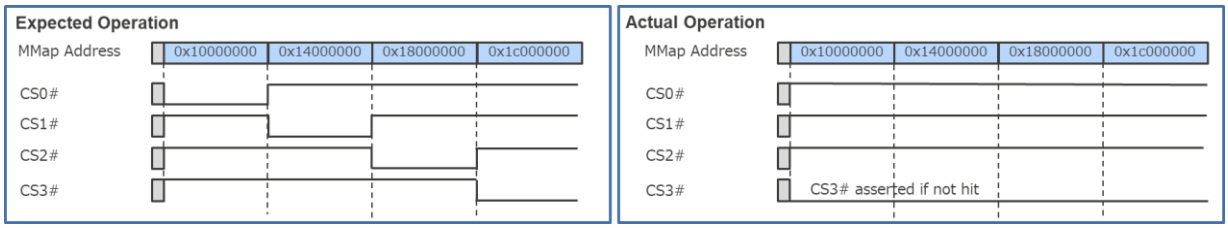
3. Issue and condition

QSPI controller in RZ/N1 assumes to receive 0 based address. On the other hand, the QSPI controller receives 32 bit width memory mapped address including offset address from NoC (Network-on-Chip) directly. Consequently, following 3 issues happen.

i. AHB decode function issue

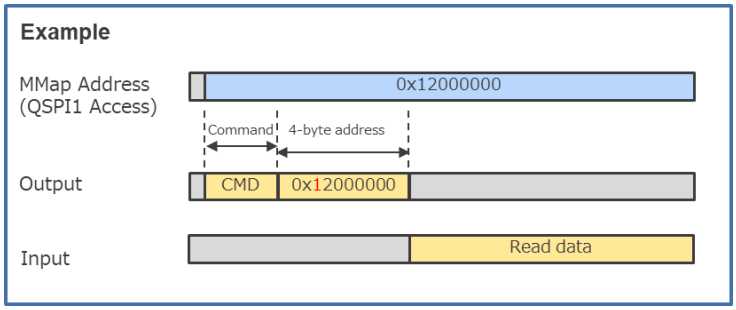
AHB decode function that switches external chip select (CS) pin by decoding address input doesn't work correctly. Timing chart below shows an example case when each CS size is set to 64MB and AHB decode function is enabled.



MMap Address = Memory Mapped Address

ii. 4-byte address output issue

In case of using more than 16MB QSPI device, 4-byte addressing is required. Since QSPI device which can be supported in RZ/N1 series is 256MB at maximum, MSB 4-bits are fixed to 4'b0 normally. However, they are reflected memory mapped address [31:28]. If QSPI device used ignores MSB 4bits, then it is no issue. But it is possible that QSPI device doesn't work correctly depending on the specification of QSPI.



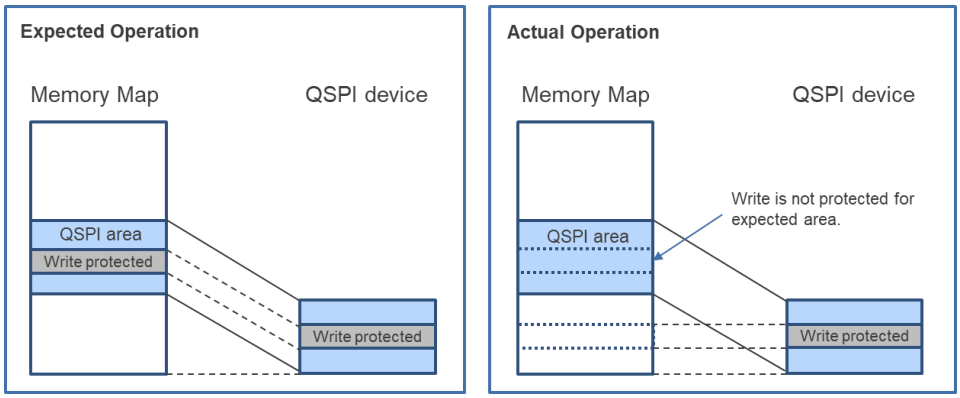
Address reflected to MSB 4-bits

QSPI1 area: 0x1

QSPI2 area: 0xA (RZ/N1S 324pin only)

iii. Write protect function issue

Write protect function of QSPI controller works for memory mapped address including offset address for QSPI area. Since QSPI controller compares write address with preset write protected area without considering offset address, write protect function doesn't work correctly for the expected area when write protected area is set based on QSPI device address.



4. Workaround

Workaround for I, ii and iii are shown below.

i. AHB decode function issue

Disable the AHB decode function and use chip select line register.

- AHB decode enable bit (config_reg.enable_ahb_decoder_fld) = 0
- Use Chip select line(config_reg.periph_cs_lines_fld)
  - Case1 config_reg.periph_sel_dec_fld = 0:

    Only 1 of 4 selects QUAD_CS_N[3:0] is active according to periph_cs_lines_fld

    xxx0b：QUAD_CS_N[3:0]＝1110b

    xx01b：QUAD_CS_N[3:0]＝1101b

    x011b：QUAD_CS_N[3:0]＝1011b

    0111b：QUAD_CS_N[3:0]＝0111b

    1111b：QUAD_CS_N[3:0]＝1111b（No CS selected)
  - Case2 config_reg.periph_sel_dec_fld = 1:

    QUAD_CS_N[3:0] is directly asserted according to periph_cs_lines_fld

ii. 4-byte address output issue

By using remap address function, it is possible to output an address without memory map offset.

- Set remap_addr_reg

  QSPI1 area: 0xF0000000

  # 0x10000000(base) + 0xF0000000(additive offset) = 0x00000000

  QSPI2 area: 0x60000000

  # 0xA0000000(base) + 0x60000000(additive offset) = 0x00000000
- config_reg. enb_ahb_addr_remap_fld = 1 # Address remap enable

iii. Write protect function issue

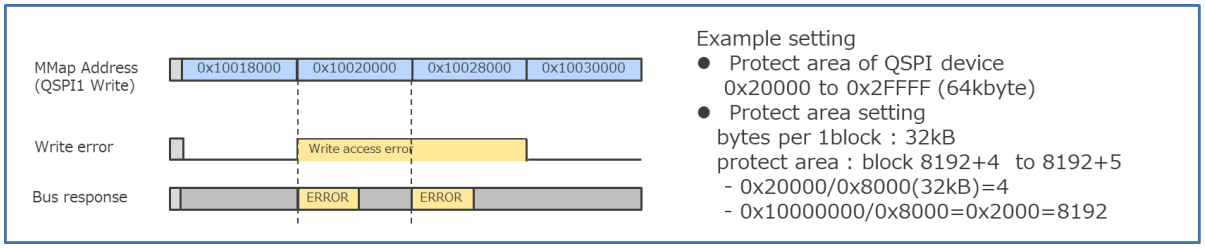
The write protect function is controlled based on the memory mapped address input to QSPI controller. Therefore it is necessary to take into account either address offset of memory mapped address, or address offset cancel by the address remap function.

Type1: Adding address offset to the write protection register

Add corresponding offset value to xxx_wr_prot_reg

Ex.） QSPI1 offset：0x10000000, block size 32 kbytes(0x8000)

Add 0x10000000/0x8000 = 0x2000(8192) to xxx_wr_prot_reg



Type2: Cancel address offset by address remap function

- Set remap_addr_reg

  QSPI1 area: 0xF0000000

  # 0x10000000(base) + 0xF0000000(additive offset) = 0x00000000

  QSPI2 area: 0x60000000

  # 0xA0000000(base) + 0x60000000(additive offset) = 0x00000000

- config_reg. enb_ahb_addr_remap_fld = 1 # Address remap enable

5. Sample driver

Sample driver provided by Renesas is not updated because it doesn’t support corresponding functions.