Microcontroller Technical Information

QB-78K0RIX3 (Old Name: QB-78K0RKX3L) In-Circuit Emulator for 78K0R/KC3-L, KD3-L, KE3-L, IB3, IC3, ID3, IE3 Usage Restrictions	Document No.	ZBG-CD-10-0007		1/2
	Date issued	January 25, 2010		
	Issued by	Development Tool Solution Group Multipurpose Microcomputer Systems Division Microcomputer Operations Unit NEC Electronics Corporation		
Related documents QB-78K0RIX3 User's Manual: U19228EJ1V0UM00 QB-78K0RIX3 (Old Name: QB-78K0RKX3L) In-Circuit Emulator for 78K0R/KC3-L, KD3-L, KE3-L, IB3, IC3, ID3, IE3 Upgrade: ZBG-CD-10-0008	Notification classification	√	Usage restriction	
			Upgrade	
			Document modification	
			Other notification	

1. Affected product

Product	Outline	Control Code[Note]
QB-78K0RIX3 (Old name: QB-78K0RKX3L)	In-circuit emulator for 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/IB3, 78K0R/IC3, 78K0R/ID3, 78K0R/IE3	A, B, C, D

Note The control code is the second digit from the left in the 10-digit serial number. To see if the product has been upgraded, click the ID78K0R-QB **Help** menu, select **About**, and then check the control code. *X* in **IECUBE **** *X* F/W: V*.**** is the control code.

2. New restriction

Restriction No. 9 has been added. See the attachment for details.

3. Workarounds

See the attachment for details.

4. Modification schedule

Products in which No. 9 is corrected are scheduled for release as follows:

Upgrade for already shipped products: Available from January 25, 2010

Date when the upgrade file is posted on the Development Tools Download webpage: January 25, 2010

Newly shipped products (control code: E): Shipments as of January 29, 2010

* Note that this schedule is subject to change without notice. For the detailed release schedule of modified products, contact an NEC Electronics sales representative.

5. List of restrictions

See the attachment.

6. Document revision history

QB-78K0RIX3 (Old Name: QB-78K0RKX3L) In-Circuit Emulator for 78K0R/KC3-L, KD3-L, KE3-L, IB3, IC3, ID3, IE3 - Usage Restrictions

Document Number	Issued on	Description
ZBG-CD-08-0041	September 18, 2008	1st edition. Addition of restrictions No. 6 to No. 8
ZBG-CD-10-0007	January 25, 2010	Addition of restriction No. 9

Operating Precautions for QB-78K0RIX3

This document describes the restrictions applicable to this emulator. Note that some restrictions have been corrected in later control codes.

See the following documents for the restrictions related to the target device:

- User's manual of target device
- Restrictions notification document for target device

Also see the user's manual for cautions on using the emulator.

1. Product Version

The product versions of NEC Electronics in-circuit emulators are indicated by a control code. The control code is the second digit from the left in the 10-digit serial number. To see if the product has been upgraded, click the ID78K0R-QB **Help** menu, select **About**, and then check the control code.

In Figure 2, ***X*** in **IECUBE **** *X* F/W: V*.**** is the control code.

Figure 1. Checking the Control Code (Label on QB-78K0RIX3)

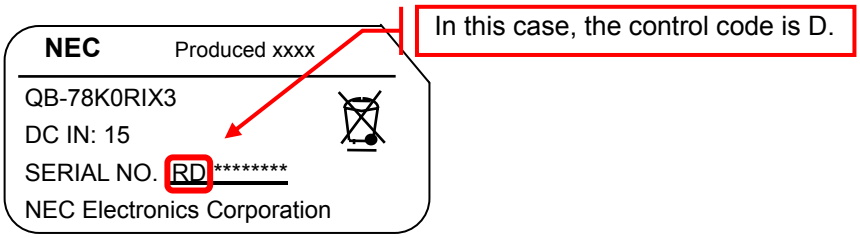
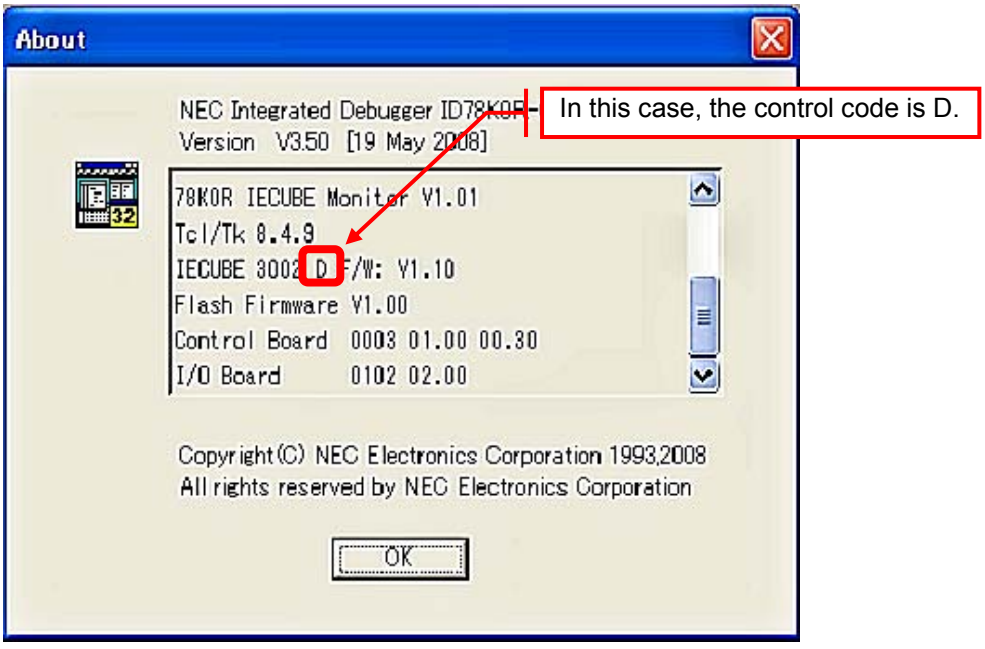


Figure 2. Checking the Control Code (ID78K0R-QB)



2. Restrictions

2.1 List of restrictions

No.	Restrictions	Control Code			
		A	B	C	D
1	Self-programming	×	×	○	○
2	Interrupt function for key-return (applicable when the target device is 78K0R/Kx3-L)	×	○	○	○
3	P73/TXD0/TO10 pin (only applicable to 38-pin MC packages)	×	○	○	○
4	Comparator interrupt function	×	×	○	○
5	Count clock for timer array unit	×	×	×	○
6	Restriction on trace data when an interrupt occurs (1)	×	×	×	○
7	Program execution on RAM	×	×	×	○
8	A break during division operation	×	×	×	○
9	Restriction on trace data when an interrupt occurs (2)	×	×	×	×

–: Not relevant, ×: Applicable, ○: Corrected

2.2 Restriction details

No. 1 Self-programming

Description:

Self-programming is not supported.

Workaround:

There is no workaround.

Correction:

This issue has been corrected in QB-78K0RIX3 with control code C.

No. 2 Interrupt function for key-return (applicable when the target device is 78K0R/Kx3-L)

Description:

The interrupt function for key-return does not operate.

Workaround:

There is no workaround.

Correction:

This issue has been corrected in QB-78K0RIX3 with control code B.

No. 3 P73/TXD0/TO10 pin (only applicable to 38-pin MC packages)

Description:

The P73/TXD0/TO10 pin can be used for reading and writing to SFRs, but its port function and alternate function do not operate.

Workaround:

There is no workaround.

Correction:

This issue has been corrected in QB-78K0RIX3 with control code B.

No. 4 Comparator interrupt function

Description:

When a comparator interrupt function is used, interrupt requests are issued continuously while an overvoltage is being detected.

In normal operation, an interrupt request is issued only once upon detection of overvoltage.

Workaround:

There is no workaround.

Correction:

This issue has been corrected in QB-78K0RIX3 with control code C.

No. 5 Count clock for timer array unit

Description:

A subsystem clock whose frequency is divided by 4 cannot be used as a count clock for a timer array unit.

Workaround:

There is no workaround.

Correction:

This issue has been corrected in QB-78K0RIX3 with control code D.

No. 6 Restriction on trace data when an interrupt occurs (1)

Description:

If a read access or write access is performed immediately before occurrence of an interrupt, this access might not be reflected to the trace result.

Workaround:

There is no workaround.

Correction:

This issue has been corrected in QB-78K0RIX3 with control code D.

An example of trace data before and after the correction of this restriction is shown below.

A read access by this MOV instruction is not reflected to the trace result.

Before correction:

```
_ A 131064 0:00:00.516 208 000 01065   AA02    M1                                  MOVW AX,[DE+2H]
_ A 131065 0:00:00.516 209 000                          F3FFE         9700  W
_ A 131066 0:00:00.516 209 500 0002E   4A01FF  VECT    F3FFC         1067  W
_ A 131067 0:00:00.516 211 500 0014A   84      M1                                    INC  E
_ A 131068 0:00:00.516 212 000 0014B   4C0F    M1                                    CMP  A,#0FH
_ A 131069 0:00:00.516 212 500 0014D   8A02    M1                                    MOV  A,[DE+2H]
_ A 131070 0:00:00.516 213 000                          F450D   83          R
```

This line shows the result of the read access by "MOVW AX, [DE+2H]".

A read access by this MOV instruction is reflected to the trace result.

After correction:

```
_ A 131063 0:00:00.258 053 000 01065   AA02    M1                                  MOVW  AX,[DE+2H]
_ A 131064 0:00:00.258 053 500                          F450C   8312        R
_ A 131065 0:00:00.258 054 000                          F3FFE         9700  W
_ A 131066 0:00:00.258 054 500 0002E   4A01FF  VECT    F3FFC         1067  W
_ A 131067 0:00:00.258 056 500 0014A   84      M1                                    INC  E
_ A 131068 0:00:00.258 057 000 0014B   4C0F    M1                                    CMP  A,#0FH
_ A 131069 0:00:00.258 057 500 0014D   8A02    M1                                    MOV  A,[DE+2H]
_ A 131070 0:00:00.258 058 000                          F450D   83          R
```

No. 7 Program execution on RAM

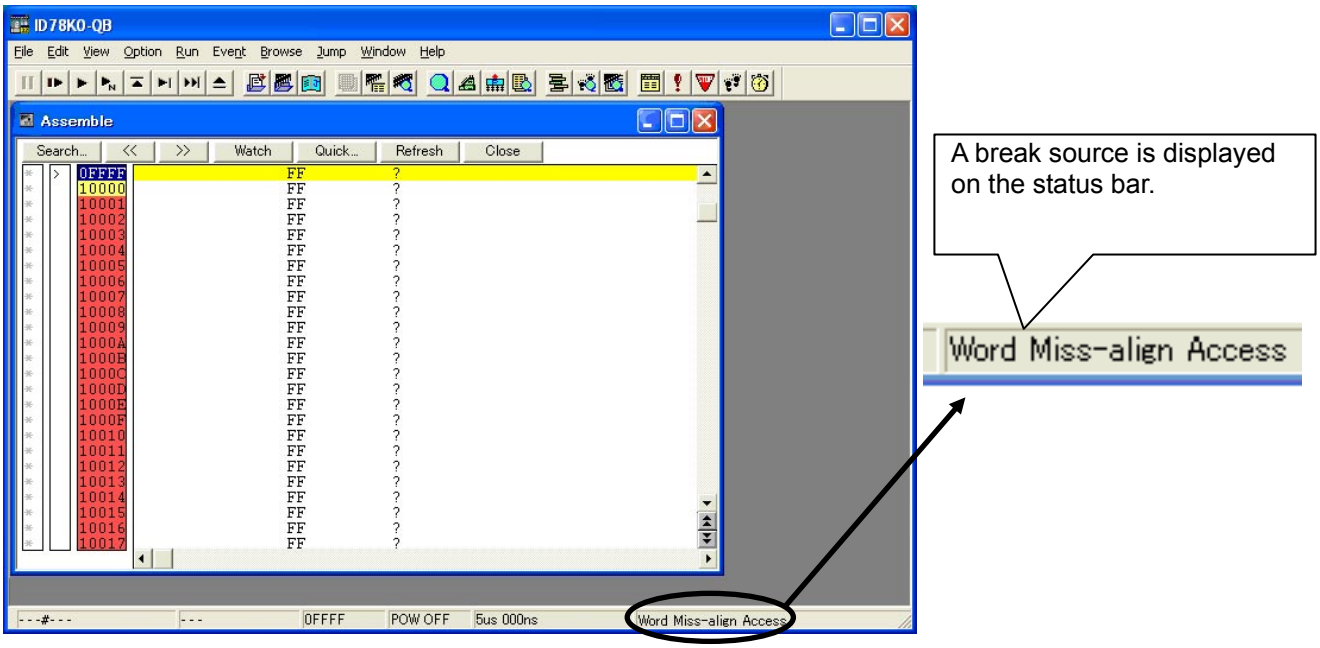
Description:

When a branch instruction is executed on RAM and if the branch destination is an odd address located in RAM, a fail-safe break due to a word misalign access occurs.

Workaround:

Clear the check box for **Word Miss-align Access** in the **Fail-Safe Break** dialog box in the ID78K0R-QB.

A break source can be checked in the status bar in the ID78K0R-QB, as shown below.



Correction:

This issue has been corrected in QB-78K0RIX3 with control code D.

No. 8 A break during division operation

Description:

If a break occurs in a program in the 16th clock cycle after a division operation is started (DIVST = 1), the operation result might be incorrect.

Workaround:

Do not set breaks for the division operation.

Correction:

This issue has been corrected in QB-78K0RIX3 with control code D.

No. 9 Restriction on trace data when an interrupt occurs (2)

Description:

If interrupt servicing is executed under a specific condition, the trace result might be incorrect.

Although the correct trace result is not displayed, the instructions are executed correctly. The following describes the detailed condition and operations:

Condition:

Execution jumps to an interrupt vector immediately after executing one of the following instructions:

(1) `MOVW SP, #word`

(2) `MOVW SP, AX`

(3) `ADDW SP, #byte`

(4) `SUBW SP, #byte`

If the instruction fetches data from the ROM, the displayed trace result is incorrect if any instruction from (1) to (4) is executed.

If the instruction fetches data from the RAM, the displayed trace result is incorrect if instruction (3) or (4) is executed.

Operation:

If execution jumps to an interrupt vector immediately after executing one of the above instructions, the instruction that follows the above instructions is not supposed to be executed or displayed in the trace result. However, due to this problem, the following items are displayed in the trace result:

- The instruction that follows the above instructions
- The incorrect vector address

Workaround:

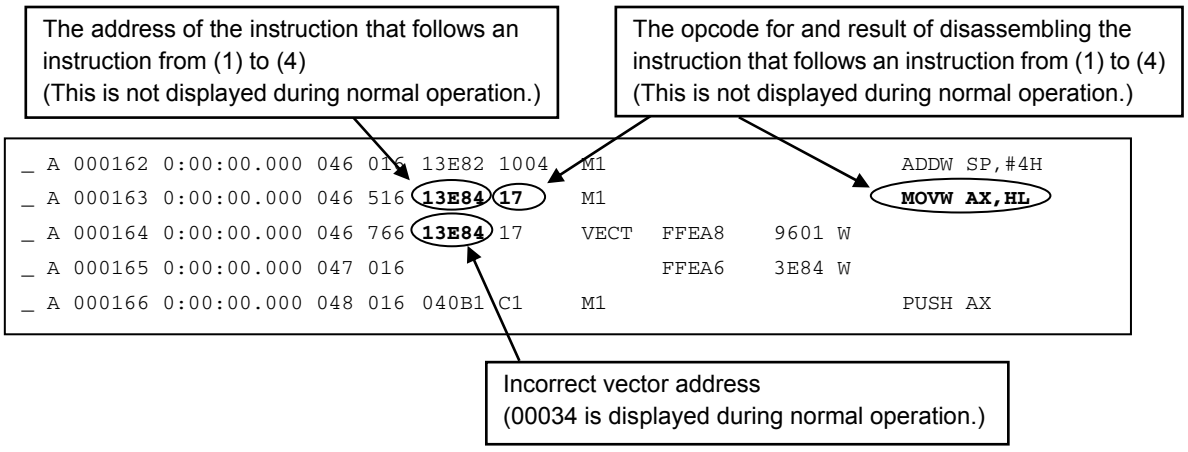
There is no workaround.

Correction:

This issue will be corrected in the next revision.

An example of trace data before and after correcting this restriction is shown below.

Before correction:



After correction: