Customer Notification

QB-70F3534-PD

In-Circuit-Emulator

Operating Precautions

Target Device

µPD70F3522-26, 35-37, V850E2/DX4

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A) Table of Operating Precautions

No.	Outline		QB-70F3534-PD			
		Rev.	**A**	**B**	**C**	**D**
		Date	**10-Dec 2009**	**10-Mar 2010**	**15-Jun 2010**	**04-Oct 2011**
		HW Version	**V1.00**	**V2.20**	**V3.10**	**V4.00**
		70F3534	**DS1.0**	**DS2.0**	**DS2.2**	**n/a**
		70F3534A	**n/a**	**n/a**	**n/a**	**ES1.0**
1	Tool status is DS		Y	N	N	N
2	Trace not supported		Y	N	N	N
3	PLL 0/1/2 not working correctly		Y	N	N	N
4	POC not supported		Y	Y	N	N
5	POC not supported when PWGDEN = 0 and PWRGOOD = L		Y	Y	Y	N
6	LVI levels are higher than for device		Y	Y	Y	N
7	VLVF not supported (Remaining limitation)		Y	Y	Y	Y
8	Ports supplied by E0VDD fixed to 5.5V of internal power supply		Y	N	N	N
9	WAKE pin is not Hi-Z during RESET		Y	Y	Y	Y
10	LCD segment pin allocation differs between device revisions		Y	Y	Y	N
11	RTC clock selector differs between device revisions		Y	Y	Y	N
12	LVI level 3.1V is not available		N	N	N	Y
13	REG1VDD must remain powered at all times when emulating devices		Y	Y	Y	Y

N: Not applicable

Y: Applicable

Note: The control code is the second letter from the left of the 10 digit serial number or in case of update the latest control code is mentioned on the version up sticker.

B) Description of Operating Precautions

No. 1	Tool status is DS
	Details Tool test coverage is below 60%. *Workaround* None.

No. 2	POC not supported
	Details When the supply voltage REG0VDD drops below the POC (power-on-clear) threshold voltage, the debugger will hang. *Workaround* None.

No. 3	Trace not supported
	Details None. *Workaround* None.

No. 4	PLL 0/1/2 not working correctly
	Details Maximum PLL frequency is up to 40 MHz. *Workaround* None.

No. 5	POC not supported when PWGDEN = 0 and PWRGOOD = L
	Details If the flash mask option PWGDEN is set to 0 and the pin PWRGOOD is at a low-level during release of the POC condition (i.e. when REG0VDD rises above the POC threshold voltage) the device will not start up. *Workaround* Clamp the pin PWRGOOD to H. As this pin's function is disabled, the level should not be of importance.

No. 6	LVI levels are higher than for device
	Details The LVI levels (set in the SFR LVICNT) are higher in the tool than in the device. The difference is approx. 0.18V. E.g. if the LVI would trigger at 3.50V in the device, it will trigger at 3.68V on the tool. *Workaround* None.

No. 7	VLVF not supported
	Details The VLVF flag is not supported. Even if REG0VDD is below the threshold voltage, the flag's value is not affected. *Workaround* None.

No. 8	Ports supplied by E0VDD fixed to 5.5V of internal power supply
	Details Following ports are effected: P0, JP0, VCMPIN, WAKE, PWRGOOD, FLMD0 *Workaround* None.

No. 9	WAKE pin is not Hi-Z during RESET
	Details The behavior of the WAKE pin during an external RESET was re-specified. Newer device versions do not drive the WAKE pin during RESET (i.e. Hi-Z). The tool drives it at all times, even during RESET. Also, the buffer characteristics and timings will differ from the device. *Workaround* None.

No. 10	LCD segment pin allocation differs between device revisions

Details
The mapping of the LCD segment functions differs between device revisions.
The tool has this configuration:
- JP0.4/SEG13
- JP0.5/SEG12

Newer device revisions have this configuration:
- JP0.4/SEG12
- JP0.5/SEG13

Workaround
a) The target hardware may be adapted to the swapped segment lines.

b) The segments may be swapped in the layout of the LCD macro (software solution).

No. 11	RTC clock selector differs between device revisions

Details
The mapping of the RTC clock selector (AWO_09) differs between device revisions.
The tool has this configuration:
ID=1 is used for the low speed ring oscillator.
Newer device revisions have this configuration:
ID=10 (non-standard) is used for the low speed ring oscillator.

Workaround
Use the corresponding ID (software solution).

No. 12	LVI level 3.1V is not available

Details
When setting the LVI to a level of 3.1V, it will not react, even if the voltage drops below this voltage.

Workaround
None.

No. 13	REG1VDD must remain powered at all times when emulating devices

Details
This item only applies when emulating one of the following devices:
uPD70F3522/23/24/25/26 when using a version of firmware prior to E1.00s
The device allows the supply pins REG1VDD0..2 to be turned off when the WAKE pin is not driving a High level (e.g. during sleep mode or reset). The tool does not allow this condition. Please keep these pins powered at all times to work with the tool.

Workaround
1) Update the firmware version to E1.00s (or later), or
2) Modify target hardware to supply REG1VDD0..2 at all times.

C) Valid Specification

Item	Date published	Document No.	Document Title
1	September 2012	R20TU0018ED0300	This document
2	April 2010	EEDT-CD-0423-2.0	Preliminary User's Manual

D) Revision History

Item	Date published	Document No.	Comment
1	December 2009	EEDT-OP-0044-1.0	1st release
2	February 2010	EEDT-OP-0044-2.0	Update
3	March 2010	EEDT-OP-0044-3.0	Tool reached ES-level
4	March 2010	EEDT-OP-0044-3.1	Update
5	April 2010	EEDT-OP-0044-3.2	New company name
6	June 2010	EEDT-OP-0044-4.0	Update
7	August 2010	R20TU0018ED0100	Update, items 5+6 separated, items 9-11 added
8	October 2011	R20TU0018ED0200	Update (new emulation chip), item 12 added
9	September 2012	R20TU0018ED0300	Minimum firmware version specification (item 13)

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