To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A657A/E	Rev.	1.00
Title	Prohibition of Interrupts during Programming/Erasing in User Program Mode		Information Category	Technical Notification		
Applicable Product	SH7211 Group	Lot No. All lots	Reference Document	SH7211 Group Hardware Manual Rev.2.00 (REJ09B0344-0200)		

We would like to inform you that some corrections have been made to the SH7211 Group Hardware Manual due to additional restrictions on programming and erasing in user program mode. Please refer to the following for details.

[Correction**]**

Page 894, Section 21 Flash Memory

21.2.6 Programming/Erasing Interface, (4) Programming/Erasing Execution, lines 11 and 12

[Before Change]

There are limitations and notes on the interrupt processing during programming/erasing. For details, see section 21.7.2, Interrupts during Programming/Erasing.

[After Change]

No interrupts (NMI, IRQ or any other kind) are to be generated during programming/erasing.

The following correction has been made to descriptions under (2) Interrupts during Programming/Erasing, 21.7.2 Interrupts during Programming/Erasing, Section 21 Flash Memory.

[Before Change]

Though an interrupt processing can be executed at realtime during programming/erasing of the downloaded on-chip program, the following limitations and notes are applied.

1. When flash memory is being programmed or erased, both the user MAT and user boot MAT cannot be accessed. Prepare the interrupt vector table and interrupt processing routine in on-chip RAM or external memory. Make sure the flash memory being programmed or erased is not accessed by the interrupt processing routine. If flash memory is read, the read values are not guaranteed. If the relevant bank in flash memory that is being programmed or erased is accessed, the error protection state is entered, and programming or erasing is aborted. If a bank other than the relevant bank is accessed, the error protection state is not entered but the read values are not guaranteed.
2. Do not rewrite the program data specified by the FMPDR parameter. If new program data is to provided by the interrupt processing, temporarily save the new program data in another area. After confirming the completion of programming, save the new program data in the area specified by FMPDR or change the setting in FMPDR to indicated the other area in which the new program data was temporarily saved.
3. Make sure the interrupt processing routine does not rewrite the contents of the flash-memory related registers or data in the downloaded on-chip program area. During the interrupt processing, do not simultaneously perform download of the on-chip program by an SCO request or programming/erasing.
4. At the beginning of the interrupt processing routine, save the CPU register contents. Before returning from the interrupt processing, write the saved contents in the CPU registers again.
5. When a transition is made to sleep mode or software standby mode in the interrupt processing routine, the error protection state is entered and programming/erasing is aborted.
   If a transition is made to the reset state, the reset signal should only be released after providing a reset input over a period longer than the normal 100 μs to reduce the damage to flash memory.

[After Change]

No interrupts (NMI, IRQ, or any other kind) are to be generated during programming/erasing of the downloaded on-chip program.

The following corrections have been made to item 5 under 21.8.2 Areas for Storage of the Procedural Program and Data for Programming, Section 21 Flash Memory.

[Before Change]

The flash memory is not accessible during programming/erasing operations. Therefore, the programming/erasing program must be downloaded to on-chip RAM in advance. Areas for executing each procedure program for initiating programming/erasing, the user program at the user branch destination for programming/erasing, the interrupt vector table, and the interrupt processing routine must be located in on-chip memory other than flash memory or the external address space.

[After Change]

The flash memory is not accessible during programming/erasing operations. Therefore, the programming/erasing program must be downloaded to on-chip RAM in advance. Areas for executing each procedure program for initiating programming/erasing and the user program at the user branch destination for programming/erasing must be located in on-chip memory other than flash memory or the external address space.

The row *Interrupt processing routine* of table 21.17 (1) Usable Area for Programming in User Program Mode in Section 21 Flash Memory has been deleted.

[Before Change]

Table 21.17 (1) Usable Area for Programming in User Program Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT
Interrupt processing routine	✓	X	✓	✓	

[After Change]

Table 21.17 (1) Usable Area for Programming in User Program Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT

Deletion of one row

The row *Interrupt processing routine* of table 21.17 (2) Usable Area for Erasure in User Program Mode in Section 21 Flash Memory has been deleted.

[Before Change]

Table 21.17 (2) Usable Area for Erasure in User Program Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT
Interrupt processing routine	✓	X	✓	✓	

[After Change]

Table 21.17 (2) Usable Area for Erasure in User Program Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT

Deletion of one row

The row *Interrupt processing routine* of table 21.17 (3) Usable Area for Programming in User Boot Mode in Section 21 Flash Memory has been deleted.

[Before Change]

Table 21.17 (3) Usable Area for Programming in User Boot Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User Boot MAT	External Space	User Boot MAT	Embedded Program Storage Area
Interrupt processing routine	✓	X	✓	✓	

[After Change]

Table 21.17 (3) Usable Area for Programming in User Boot Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User Boot MAT	External Space	User Boot MAT	Embedded Program Storage Area

Deletion of one row

The row *Interrupt processing routine* of table 21.17 (4) Usable Area for Erasure in User Boot Mode in Section 21 Flash Memory has been deleted.

[Before Change]

Table 21.17 (4) Usable Area for Erasure in User Boot Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User Boot MAT	External Space	User Boot MAT	Embedded Program Storage Area
Interrupt processing routine	✓	X	✓	✓	

[After Change]

Table 21.17 (4) Usable Area for Erasure in User Boot Mode

Item	Storable/Executable Area			Selected MAT	
	On-Chip RAM	User Boot MAT	External Space	User Boot MAT	Embedded Program Storage Area

Deletion of one row