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April 1st, 2010
Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Date: Feb.02.2010

Product Category	MPU & MCU		Document No.	TN-16C-A182A/E	Rev.	1.00
Title	A Programming Note on Wait Mode and Stop Mode in the R32C/100 Series		Information Category	Technical Notification		
Applicable Product	R32C/100 Series	Lot No.	Reference Document			

1. Note

This document describes possible errata with the R32C Series in which the device exits wait mode or stop mode immediately without any interrupt if either of the following operations is performed:

- Setting the interrupt request flag[*1] for an interrupt to 0,
- Setting the interrupt request level[*2] for that interrupt to the same level as processor interrupt priority level (IPL) or lower.

Note that the above operations are dependent on the following three conditions:

(1) The I flag is 0 (interrupt disabled),
(2) The interrupt request level for the interrupt is higher than the IPL,
(3) The interrupt request flag for the interrupt is 1.

*1. Interrupt request flag: The IR bit in the interrupt control register
*2. Interrupt request level: Setting values of bits ILVL2 to ILVL0 in the interrupt control register

2. Solution

2.1 Wait Mode

To enter wait mode, follow the procedure below. The interrupt control register should be set according to the description in the hardware manual.

• Steps before entering wait mode

(1) Set the I flag to 0.
(2) Set the interrupt request level for each interrupt source (interrupt number from 1 to 127) to 0, if its interrupt request level is not 0.
(3) Perform a dummy read of any interrupt control registers.
(4) Set the processor interrupt priority level (IPL) in the flag register (FLG) to 0.
(5) Enable interrupts temporarily by executing the following instructions:
FSET I
NOP
NOP
FCLR I
(6) Set the interrupt request level for the interrupt to exit wait mode.
Do not rewrite the interrupt control register after this step.
(7) Set the IPL in the flag register.
(8) Set the interrupt priority level for resuming to the same level as the IPL.
Interrupt request level for the interrupt to exit wait mode > IPL = Interrupt priority level for resuming.
(9) Change the current operation mode to another[*1] to move to wait mode.[*2]
(10) Set the I flag to 1.
(11) Execute the WAIT instruction.

*1. Low speed mode and low power mode are applicable. PLL self-oscillation mode is also available in some products.
*2. When the oscillator stop detection is used, set the CM20 bit in the CM2 register to 0 (oscillator stop detection disabled). This bit setting may be done any timing of the steps above but must be completed before the main clock stops.

2.2 Stop Mode

To enter stop mode, follow the procedure below. The interrupt control register should be set according to the description in the hardware manual.

• Steps before entering stop mode

(1) Set the I flag to 0.
(2) Set the interrupt request level for each interrupt source (interrupt number from 1 to 127) to 0, if its interrupt request level is not 0.
(3) Perform a dummy read of any interrupt control registers.
(4) Set the IPL in the flag register to 0.
(5) Enable interrupts temporarily by executing the following instructions:
FSET I
NOP
NOP
FCLR I
(6) Set the interrupt request level for the interrupt to exit stop mode.
Do not rewrite the interrupt control register after this step.
(7) Set the IPL in the flag register.
(8) Set the interrupt priority level for resuming to the same level as the IPL.
Interrupt request level for the interrupt to exit stop mode > IPL = Interrupt priority level for resuming.
(9) Change the base clock to either the main clock divided by 256 (f256) or the on-chip oscillator clock divided by 4 (fOCO4).*1
(10) Set the I flag to 1.
(11) Execute the STOP instruction.*1

*1. When the oscillator stop detection is used, set the CM20 bit in the CM2 register to 0 (oscillator stop detection disabled).