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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RL*-A052A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Precaution of using High accuracy 1 Hz output | | Information Category | Technical Notification | | |
| Applicable Product | RL78/I1B Group<br>R5F10Mxx | Lot No.<br>All lot | Reference Document | RL78/I1B User's Manual: Hardware Rev2.00<br>R01UH0407EJ0200(Mar 2014) | | |

Precaution described below is added to the above products in the User's Manual.

List of corrections to be added in this notification

| Item | Correction Item | Applicable Page | Contents |
|---|---|---|---|
| 1-1 | 8.4.7 Clock error correction register setting procedure | P.309 | Precaution added |
| 1-2 | Figure 8-1. Real-time Clock 2 Diagram | P.281 | Incorrect descriptions revised |

Precaution is added in Gray hatched.

1-1. Precaution regarding the clock error correction register (SUBCUD) setting procedure when using the high accuracy 1 Hz output.

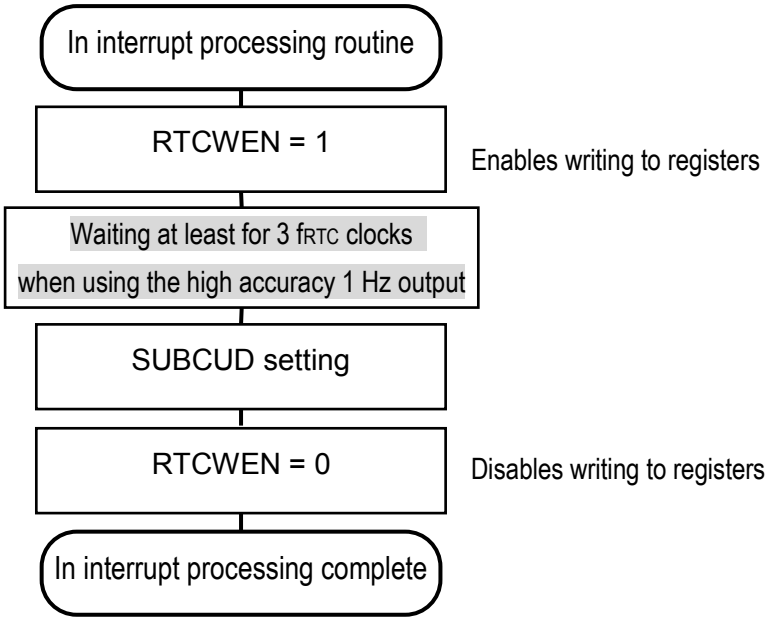
Use either of the following procedures to set the clock error correction register (SUBCUD).

In order to prevent write error to the clock register, write privilege with (2) FMCEN is recommended for rewrite of the SUBCUD register.

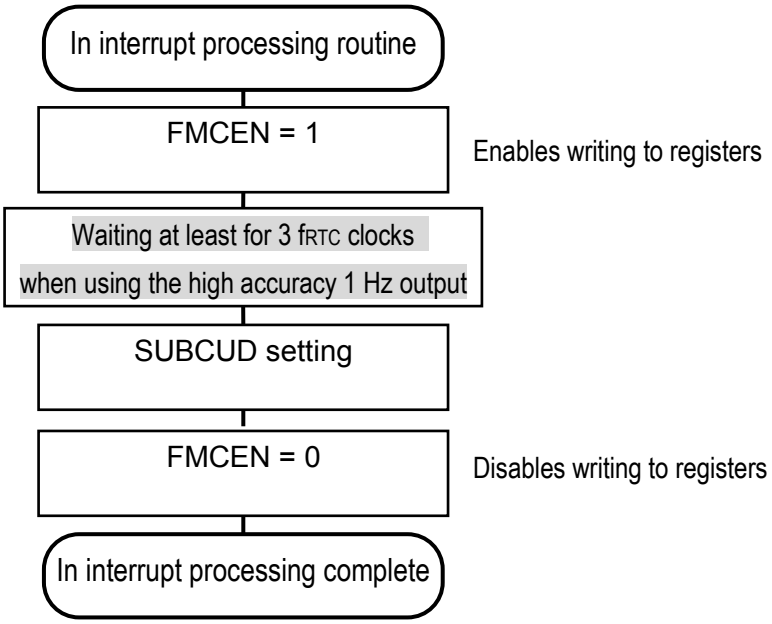
RTC correction may not be successful if there is a conflict between the SUBCUD register rewrite and correction timing. In order to prevent conflict between the correction timing and rewrite of the SUBCUD register, be sure to complete rewrite of the SUBCUD register before the next correction timing occurs (within approx. 0.5 seconds), which is calculated starting from the correction timing interrupt (INTRTIT) or periodic interrupt (INTRTC) that is synchronized with the correction timing.

When using the high accuracy 1 Hz output and rewriting the SUBCUD register, rewrite the SUBCUD register after waiting at least for 3 $f_{RTC}$ clocks.

(1) Set the clock error correction register (SUBCUD) after setting RTCWEN to 1 first. Then set RTCWEN to 0 after completion of the register setting.



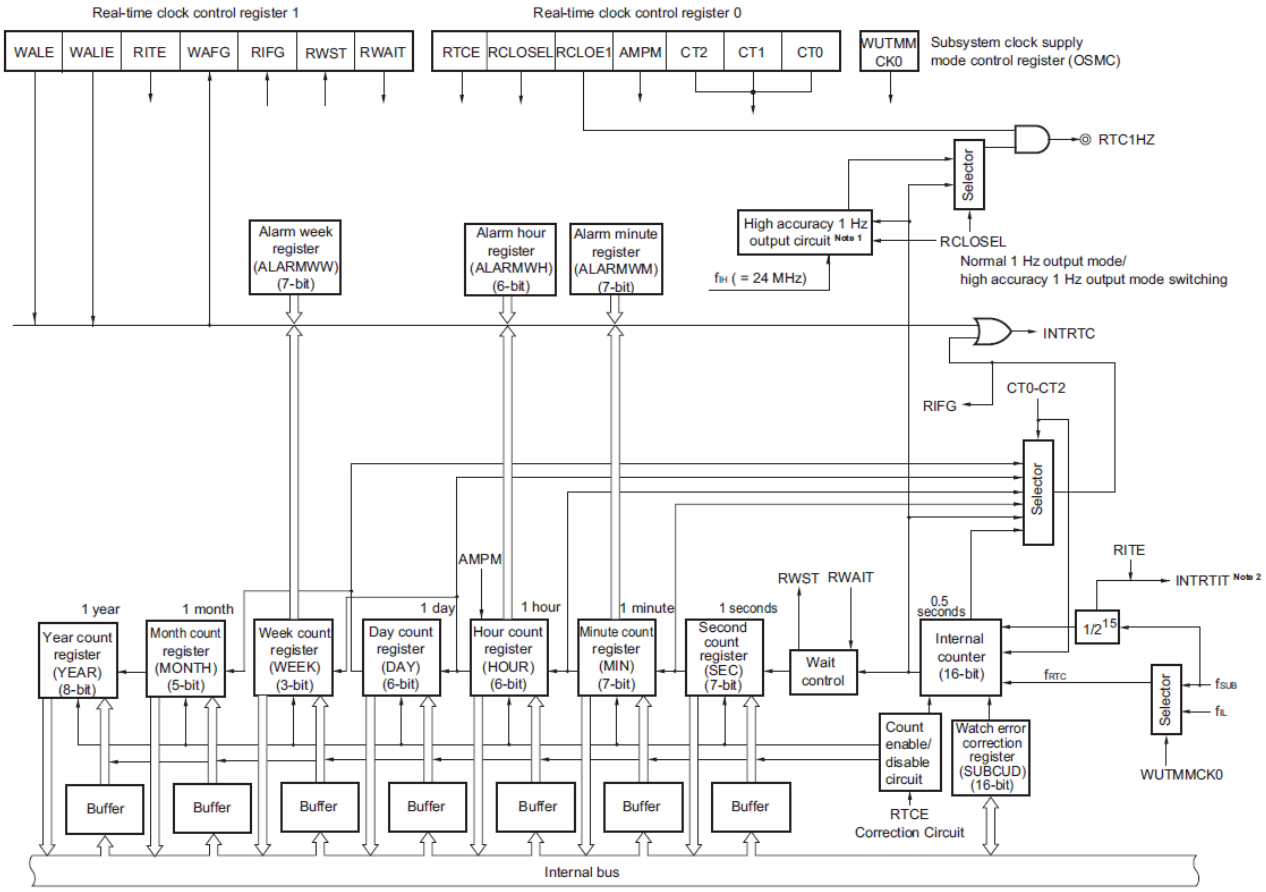

(2) Set the clock error correction register (SUBCUD) after setting FMCEN to 1 first. Then set FMCEN to 0 after completion of the register setting.



1-2. Root correction of the INTRTIT in the Real-time Clock 2 Diagram

Incorrect :

<R> **Figure 8-1. Real-time Clock 2 Diagram**



Correct:

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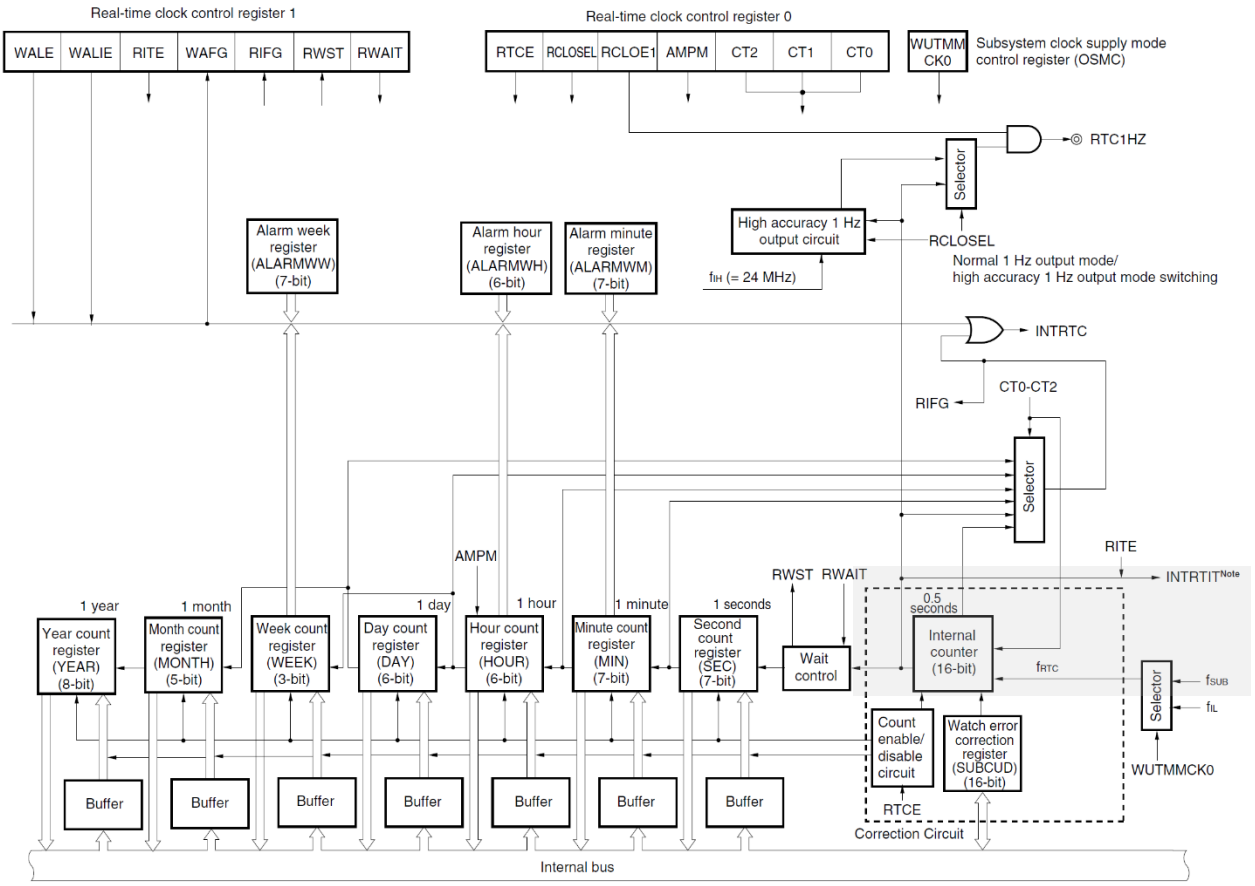
**Figure 7-1. Real-time Clock 2 Diagram**




**Note** An interrupt that indicates the timing to get the correction value from the clock error correction register (SUBCUD). The fetch timing is 1 second ($f_{SUB}$ base) interval.