RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0084B/E	Rev.	2.00	
Title	Precaution regarding interrupt during success access to peripherals sharing the same slave interfaces	of during successive bus g the same slave		Technical Notification			
Applicable Product	RA6M1 Group, RA6M2 Group, RA6M3 Group, RA6T1 Group, RA4M1 Group, RA4W1 Group	Lot No.		Refer table at the end of this document			
		All	Reference Document				

If all the conditions described below applies to your software, one of the following workarounds could be used to resolve observed unexpected software behavior:

[Condition]

All of the following conditions must be met:

- Clock frequency setting: a)

 - ICLK > PCLKx (x=A,B) (RA4M1, RA4W1) ICLK > PCLKx (x=A,B), ICLK>FCLK (RA6M1, RA6M2, RA6M3, RA6T1)
- A preceding access to the Slave interface or External bus (referred to as Access1) is followed by a subsequent access to b) the same slave interface or external bus (referred to as Access2).
- No access to other Slave interfaces and External bus between Access1 and Access2 occurs. c)
- d) An interrupt occurs on the last PCLKx/FCLK cycle of Access1.

Applicable slave interfaces and external bus:

Bus specifications (User's Manual: Hardware)

Table 15.1 for RA6M1,RA6M2,RA6M3,RA6T1, and RA4W1

Table 14.1 for RA4M1

		RA6M1/ RA6T1	RA6M2	RA6M3	RA4M1	RA4W1
Slave	Memory bus 1	-	-	-	-	-
interface	Memory bus 2	-	-	-		
	Memory bus 3	-	-	-	-	-
	Memory bus 4	-	-	-	-	-
	Memory bus 5	-	-	-		
	Internal peripheral bus 1	-	-	-	-	-
	Internal peripheral bus 3	~	~	~	~	~
	Internal peripheral bus 4	~	~	~	~	~
	Internal peripheral bus 5	~	~	~	~	~
	Internal peripheral bus 7	~	~	~	~	~
	Internal peripheral bus 8			~		
	Internal peripheral bus 9	~	~	~	-	-
External	CS area	-	-	-		
bus	SDRAM area		-	-		
	QSPI area	~	~	~		



[Precaution] Case1 : A wrong access to Access2 target register might occur when all issue conditions meet. 1) When Access2 is write operation, wrong data is written to Access2 target register temporary, then a correct value is written after the CPU returning from interrupt. 2) If Access2 target register has FIFO or flag bit clear function, it causes unintentional value write to FIFO or unnecessary read from FIFO, or unintentional flag bit clear on the register. Case2 : A wrong access might occur in interrupt service routines when all issue conditions meet. A register access to the same slave interface or external bus as Access2 in an interrupt service routine (referred to as Access3) causes an illegal operation 3) When Access3 is read operation, CPU might receive wrong data. 4) When Access3 is write operation, Access3 might not occurred in target register. 5) If Access3 target register has FIFO or flag bit clear function, these functions don't operated correctly. *These behaviors may occur in combination. Case1 ICLK Condition a) **PCLKx** Condition b) Successive access to same I/F without interrupt BUS Access1 Access2 Value of Access2 target register Condition c) In the above accesses, an interrupt occurs Access after Interrupt routine Interrupt Generated by interrupt BUS Access1 (XXX) Access2 Resume after Interrupt process Context stacking is done due to interrupt Condition d Case1-1) Value of Access2 target register Data before change Wrong Data by write operation Correct Data Without FIFO and clear function Case1-2) Value of Access2 target register Data before change with FIFO or clear function If Access2 target register has FIFO or clear function, these don't operate correctly on Access2 read/write operation Case2 ICLK Condition a) PCLKx Condition Successive access to same I/F without interrupt BUS X Access1 Access2 Condition c) Access3 to same slave interface as Access2 In the above accesses, an interrupt occurs Access during Interrupt routine Interrupt Generated by interrupt In addition, if Access3 target Case2-3,5 register has FIFO or clear BUS X Access1 Access3(Read) function, these functions Context stacking is done due to interrupt Get Wrong Data or don't operated correctly Condition d Read operation Interrupt Ű Generated by interrupt BUS X Access1 Access3(Write) Case2-4,5) Value of Access3 target register Access3 write operation isn't occurred



[Workaround]

Apply one of the following workarounds.

- 1) In your system, set clock frequency as follows ICLK = PCLKx (x=A,B) (RA4M1, RA4W1)
 - ICLK = PCLKx (x=A,B), ICLK=FCLK (RA6M1, RA6M2, RA6M3, RA6T1)
- 2) Identify in your code where successive Access1 and Access2 occurs relevant to the area where the unintended SW behavior was observed. Then insert DSB instruction between Access1 and Access2
- 3) Disable Interrupts during Access1 to Access2
- Note: Either one of the workarounds above will address the issue; therefore, choosing which one to apply will depend on your system requirements and behavior.

[Reference Documents]						
Product Group	Document Name	Revision				
RA6M1	Renesas RA6M1 Group User's Manual: Hardware	Rev.1.20				
RA6M2	Renesas RA6M2 Group User's Manual: Hardware	Rev.1.20				
RA6M3	Renesas RA6M3 Group User's Manual: Hardware	Rev.1.20				
RA6T1	Renesas RA6T1 Group User's Manual: Hardware	Rev.1.20				
RA4M1	Renesas RA4M1 Group User's Manual: Hardware	Rev.1.00				
RA4W1	Renesas RA4W1 Group User's Manual: Hardware	Rev.1.00				

