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GRADE **A**

MITSUBISHI ELECTRIC TECHNICAL NEWS

No. M16C-63-0011

Points to care about when using M16C/6N0, M16C/6N1, and M16C/6N3 groups
Status read of the CAN module

Content	Concerned
☐ Document error and correction list ■ Points to care about ☐ Know-how ☐ Others	M16C/6N0 Group M16C/6N1 Group M16C/6N3 Group

CAN module of M16C/6N0, M16C/6N1, and M16C/6N3 groups conducts status rewrite to some of the SFR (see Table 1) for CAN at a certain interval. If CPU and CAN module attempt to access to the SFR at the same time, priority is given to CPU and access from CAN module is disabled according to the specifications.

(Arbitration specification concerning concurrent access are introduced to support bit-set and bit-clear instructions – which are read-modify-write instructions – in a certain area of SFR dedicated to CAN.)

Due to this, CAN status could not be rewritten if status rewrite period of the CAN module would overlap that of CPU access constantly. (See Figure 1.)

Please note the following points so that CPU access to SFR would not synchronize with CAN module rewrite period.

(1) A wait time of 3fcan or more (Table 2) is required before CPU reads the CAN status register (see Figure 2-1).

(2) In case CPU polls the CAN status register, polling period must be longer than 3fcan (Figure 2-2).

Table 1: SFR of which status is rewritten by CAN module in a certain period

Register name	Symbol	Address	Symbol
CAN status register	C0STR C1STR (6N0 only)	0213_{16}, 0212_{16} 0233_{16}, 0232_{16}	b0 ~ 3: MBox Bit0 ~ Bit3 b4: TrmSucc b5: RecSucc b6: TrmState b7: RecState b8: ResetAck b12: BusError b13: ErrPass b14: BusOff
Time Stamp register	C0TSR C1TSR (6N0 only)	$021F_{16}$, $021E_{16}$ $023F_{16}$, $023E_{16}$	

Table 2: CAN module status rewrite period

3fcan time = 3 × Xin (original oscillation) × Division value for CAN clock (CCLK)	
(Example 1) Condition Xin 16MHz, CCLK: No division	3fcan time = 3 × 62.5 ns × 1 = 187.5 ns
(Example 2) Condition Xin 16MHz, CCLK: Divided by 2	3fcan time = 3 × 62.5 ns × 2 = 375 ns
(Example 3) Condition Xin 16MHz, CCLK: Divided by 4	3fcan time = 3 × 62.5 ns × 4 = 750 ns
(Example 4) Condition Xin 16MHz, CCLK: Divided by 8	3fcan time = 3 × 62.5 ns × 8 = 1.5 µs
(Example 5) Condition Xin 16MHz, CCLK: Divided by 16	3fcan time = 3 × 62.5 ns × 16 = 3 µs

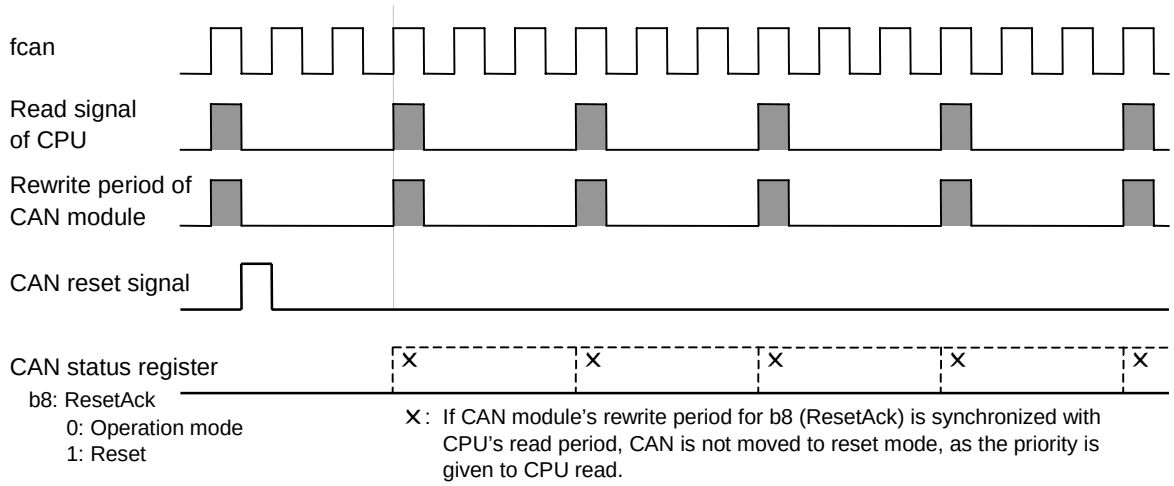

Figure 1. When CAN module's rewrite period is synchronized with CPU's read period

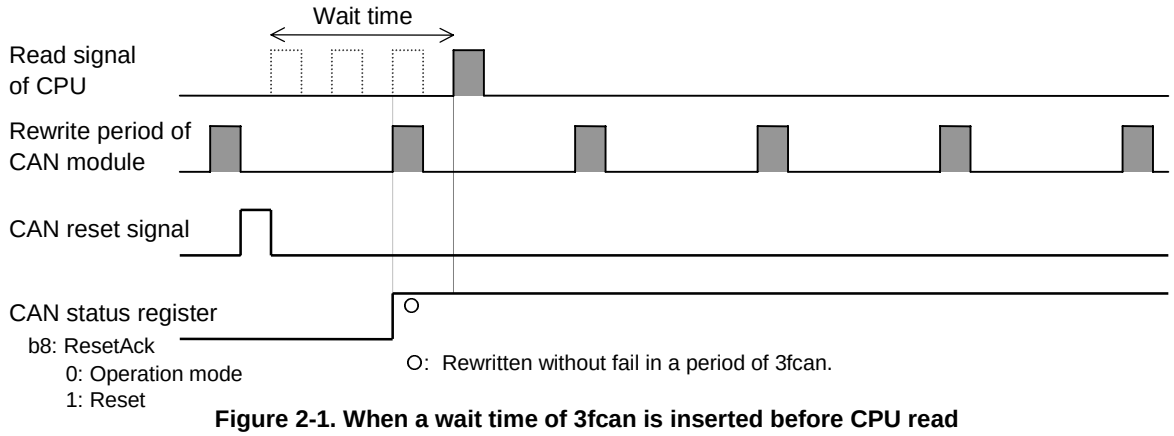

Figure 2-1. When a wait time of 3fcan is inserted before CPU read

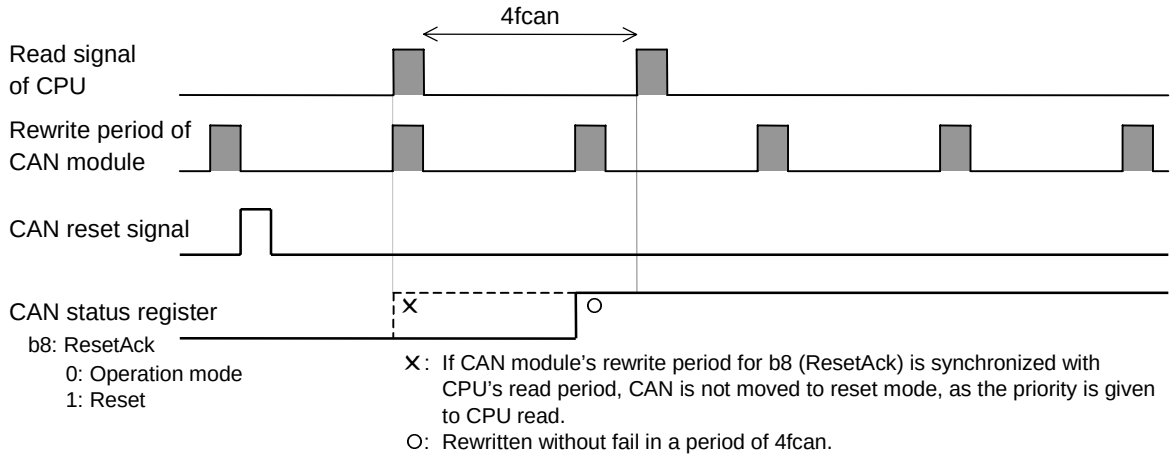

Figure 2-2. When CPU's polling period is longer than 3fcan