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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A018A/E	Rev.	1.00
Title	Point for Caution When the Port Output Enable 2 and 3 Registers (POE2 and POE3) Settings Release Pins from the High-Impedance State		Information Category	Technical Notification		
Applicable Product	RX62N Group, RX621 Group RX62T Group	Lot No. All lots	Reference Document	RX62N Group, RX621 Group User's Manual: Hardware, RX62T Group User's Manual: Hardware		

The point for caution described below applies regarding the settings of the port output enable 2 and port output enable 3 registers (POE2 and POE3), so apply the method described as a countermeasure in such cases. Furthermore, the manuals are being corrected accordingly, so details of the changes to the text are given. The corrections are explained using the RX62N Group, RX621 Group User's Manual: Hardware as an example. For the corresponding sections in other manuals, refer to Table 1, Section Numbers for the POE in Manuals (listed below).

1. Release from the High-Impedance State

1.1 Point for Caution

When the MTU pins have been placed in the high-impedance state due to output-level detection, the pins will be released from the high-impedance state either by returning them to their initial state with a reset, or by clearing the OCSR1.OSF1 or OCSR2.OSF2 flag to 0. If the OCSR1.OSF1 or OCSR2.OSF2 flag is cleared to 0 while an inactive level is not output from the MTU pins, the pins will be released from the high-impedance state even though they are in the output collision state and then enter the high-impedance state again.

1.2 Countermeasure

Ensure that clearing of the OCSR1.OSF1 or OCSR2.OSF2 flag to 0 only proceeds while the MTU complementary PWM output pins are at the inactive level.

1.3 Correction in the Manuals

The description on section 19.3.5, Release from High-Impedance State, has been revised. The revision is indicated by the red letters below.

[After correction]

MTU pins which have entered high-impedance state due to output-level detection can be released from the state either by returning them to their initial state with a reset, or by clearing the OCSR1.OSF1 or OCSR2.OSF2 flag. The output on the pins must be at the inactive level before the OCSR1.OSF1 or OCSR2.OSF2 flag becomes 0. Inactive-level outputs can be achieved by setting the MTU, GPT, and ALR1 internal registers.

Table 1 Section Numbers for the POE in Manuals

Group	Related Documents	Rev.	Control Code	Section No. for the POE
RX62N, RX621	RX62N Group, RX621 Group User's Manual: Hardware	1.30	R01UH0033EJ0130	19
RX62T	RX62T Group User's Manual: Hardware	1.30	R01UH0034EJ0130	17