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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-H8*-A435A/E	Rev.	1.00
Title	Point for Caution on Output State Retention of Port 4		Information Category	Technical Notification		
Applicable Product	H8S/2153 Group H8S/2164 Group H8S/2472, H8S/2463, H8S/2462 Group	Lot No. All lots	Reference Document	H8S/2153 Group Hardware Manual (REJ09B0384 Rev.3.00) H8S/2164 Group Hardware Manual (REJ09B0429 Rev.2.00) H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual (REJ09B0403 Rev.2.00)		

When relying on the output state retention function of port 4 in a product of the H8S/2153 Group, H8S/2164 Group, or H8S/2472, H8S/2463, H8S/2462 Group, caution is required on the following point.

1. Functions to Which the Caution Applies

Output state retention is described as follows in the parts on port 4 registers of section 8, I/O Ports, in the hardware manuals listed above.

(1) Port 4 Data Direction Register (P4DDR)

The individual bits of P4DDR specify input or output for the pins of port 4.

These bits are initialized only by a system reset, and retain their values even when an internal reset signal is generated by the WDT.

(2) Port 4 Data Register (P4DR)

P4DR stores output data for the port 4 pins.

These bits are initialized only by a system reset, and retain their values even when an internal reset signal is generated by the WDT.

When a pin of port 4 is used as an output while there is a possibility of the watchdog timer generating an internal reset, caution is required on the following point.

2. Conditions that Require Caution

(1) The possibility of an internal reset being generated by the watchdog timer

(2) A pin of port 4 being used as an output

The point for caution described in this Technical Update becomes applicable if conditions (1) and (2) are both satisfied.

3. Point for Caution on Usage

Pins of port 4 are set to the high-impedance state during the period in the reset state for an internal reset by the watchdog timer (518 cycles of the system clock). This may change the levels on pins of port 4 if they are being pulled up or pulled down.

After release from an internal reset by the watchdog timer, output pins of port 4 are returned to their states immediately before the internal reset.