Concerned Products:	**Customer Notification**	Date: April 23, 1998
		NEC-Electronics (Europe) GmbH EAD -Technical Product Support
µPD78F0988 µPD780988 µPD780986 µPD780984 µPD780983	**Bug Report**	Source Doc:
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Date of initial issue: Apr. 23rd, 98	Doc. No.: TPS-LE-B-0902
1st revision :	Doc. No.: TPS-LE

(A) BUG LIST

Bug No.	Outline	uPD78F0988			uPD78098x	
		ES V1.0	ES V2.0	ES V3.0	ES V1.0	
1	Flash memory characteristics	💣	💣	✋	No Flash	
2	AD Converter	💣	💣	💣	💣	
3	UART	✋	✓	✓	✓	

✓: No problem

✋: Bug (will be corrected by next version upgrade)

💣: Bug (restriction, not corrected by version upgrade)

(B) BUG DESCRIPTION

<table>
<tr><th>Bug No.</th><th>Outline</th><th>Description</th></tr>
<tr><td>1</td><td>Flash memory characteristics</td><td>Details
These products do not satisfy the specification with respect to the number of write / erase cycles.
<table>
<tr><td></td><td>Number of W/E Times</td><td>Operating Temperatur e</td><td>Temperatur e for Rewriting</td><td>Data Retention Time</td></tr>
<tr><td>Target spec</td><td>20 Times</td><td>-40 to + 85</td><td>0 to 40</td><td>10 years</td></tr>
<tr><td>V1.0 ES
V2.0 ES</td><td>5 to 20 Times</td><td>-40 to +85</td><td>25</td><td>No general guarantee!
The Self-writing is not available.</td></tr>
<tr><td>V3.0 ES</td><td>20 Times</td><td>-40 to + 85</td><td>0 to 40</td><td>??? years</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>2
2a

2b</td><td>A/D Converter</td><td>Details
When starting the A/D conversion with the ADCS0 bit set to “1”, the first A/D conversion value may be quite different from the expected value. Thus, use one of the following conversion values only!
When a write operation to the A/D converter control registers (ADM0, ADMS0) appears at the same time when the A/D conversion interrupt (INTAD) is generated, the A/D conversion result register (ADCR0) becomes undefined. Therefor, a read operation from ADCR0 must be performed before a write operation to ADS0 and /or ADM0 is done.</td></tr>
<tr><td>3</td><td>UART</td><td>After receiving interrupt (INTSR0 or INTSR1), ensure a sufficient wait time (t_{READ}) before reading the receiver buffer register (RXB00 or RXB01). The wait time should be at least one source clock cycle, which was selected by TPS000, TPS001 and TPS002 or by TPS010, TPS011 and TPS012 at the baud rate generator control register (BRGC00 or BRGC01).

Example: fx = 8 MHz, BRGC00 = 5AH (= 4800Bd)
For this setting, pls. wait for more than 2^5 / fx = 4us</td></tr>
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