Concerned Products:	**Customer Notification**	Date: November 10, 1999
		NEC-Electronics (Europe) GmbH EAD -Technical Product Support
µPD78P0308GF µPD78P0308GC µPD78P0308KL-T µPD78P0308YGF µPD78P0308YGC µPD78P0308YKL-T	**Bug Report**	Source Doc: SBB-T-12194
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1st edition :	Doc. No.:

(A) BUG LIST

Bug No.	Outline	78P0308(Y)GF/GC Control Code "K"	78P0308(Y)GF/GC Control Code "E" **Note 1**	78P0308(Y)GF/GC Control Code "E" **Note 2**	78P0308(Y)KL-T Control Code "I" **Note 3**	78P0308(Y)KL-T Control Code "I" **Note 4**
1	CPU operating voltage range	✸	✋	✓ Operable at VDD = 2.0 to 5.5V	✋	✓
2	LCD display data memory	✋	✓	✓	✋	✓
3	AD Converter operating voltage range	✸	✋	✓ Operable at VDD = 2.2 to 5.5V	✋	✓
4	LCD C/D supply voltage	✋	✓	✓	✋	✓

✓: No problem, anymore

✋: Limitation will be improved in next version.

✸: Bug restriction

Note 1: The devices belonging to this column have a **Control Code** xxxxExxxx **and a Date Code** earlier than "9920".

Note 2: The devices belonging to this column have a **Control Code** xxxxExxxx **and a Date Code** equal or later than "9920".

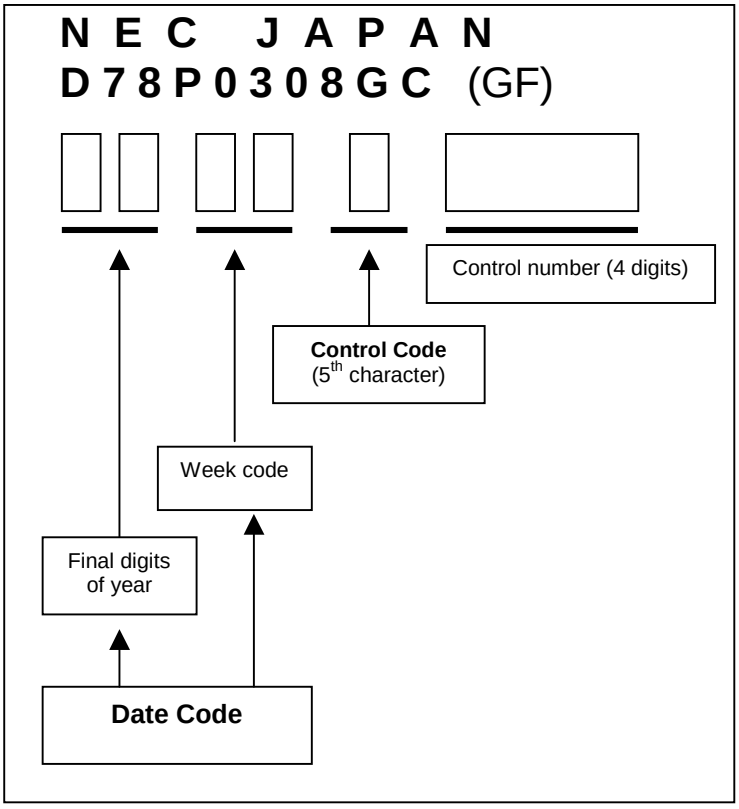
Note 3: The devices belonging to this column have a **Control Code** xxxxIxxxx **and a Date Code** earlier than "9912".

Note 4: The devices belonging to this column have a **Control Code** xxxxIxxxx **and a Date Code** equal or later than "9912".

(B) BUG DESCRIPTION

1	CPU operating voltage range	Details Make sure to use the product within the following supply voltage range. 2.7V ≤ VDD ≤ 5.5V
2	LCD display data memory	Details Do not use the instructions included on page 4 with the LCD display data memory (address FA58h to FA7Fh). The instructions may not be executed normally. However, the LCD display works normally.
3	AD Converter operating voltage range	Use the A/D converter in the condition VDD1=VDD2=AVREF=4.0 to 5.5V. In other conditions, the conversion precision may be dramatically deteriorated.
4	LCD C/D supply voltage	In the LCD display mode register (LCDM), it is not possible to select the low voltage operation. Set „0“ for LCDM register bit 3

Figure 1: uPD78P0308 Marking (Reference)



Instructions unusable for LCD Display Data Memory

Mnemonic	Operand	Mnemonic	Operand
MOV	A,!addr16 A, [DE] A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]	AND	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]
XCH	A,!addr16 A, [DE] A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]	OR	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]
MOVW	AX,!addr16	XOR	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]
ADD	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]	CMP	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]
ADDC	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]	MOV1	CY,[HL].bit [HL].bit,CY
SUB	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]	AND1	CY, [HL].bit
SUBC	A,!addr16 A, [HL] A, [HL+byte] A, [HL+B] A, [HL+C]	OR1	CY, [HL].bit
ROR4	[HL]	XOR1	CY, [HL].bit
ROL4	[HL]	SET1	[HL].bit
		CLR1	[HL].bit
		BT	[HL].bit, $addr16
		BF	[HL].bit, $addr16
		BTCLR	[HL].bit, $addr16