Concerned Products:	**Customer Notification**	Date: 17. Feb. 98
		NEC-Electronics (Europe) GmbH EAD -Technical Product Support
µPD30102 **(V_R-4102)**	**Bug Report**	Source Doc: SBB-T-8752-E, SBB-T-9063-2-E
		Author: Guido Hilker
Date of initial issue: 17. Feb. 98		Doc. No.: TPS-HE-B-6002

(A) BUG LIST

Bug No.		Outline	µPD30102					
			R1.0	R1.1	R1.2	R1.3	R1.4	R2.0
1		Sizing error in the ISA high-speed system bus memory space						✓
2		Access speed error in the ISA high-speed system bus memory space						✓
3		Audio input DMA buffer address error						✓
4		16-bit data bus mode error						✓
5		Bus hold function error		Note 2	Note 2	Note 2	Note 2	✓
6		SIU, FIR, HSP access error						✓
7		Page ROM access error		Note 2	Note 2	Note 2	Note 2	✓
8		SIR transmission error					✓	✓
9		GPIO data read error					✓	✓
10		TPX [1:0] initial status error					✓	✓
11		Touch interrupt error					✓	✓
12		PIUCMDREG bit assignment error					✓	✓
13		ADP scanning error						✓
14		CMD scanning error						✓

Bug No.		Outline	R1.0	R1.1	R1.2	R1.3	R1.4	R2.0
15		Audio output error					✓	✓
16		DMA error					✓	✓
17		Serial receiving data ready error		Note 3	Note 3	Note 3	Note 3	Note 3
18		FROM speed setting error						✓
19		QFP pin assignment error					✓	✓
20		RSTOUT pin error					✓	✓
21		SDO output error				Note 3	✓	✓
22		FIR data receiving error					✓	✓
23		PIU touch status display error					✓	✓
24		GPIO interrupt error						✓
25		Internal ISA error					✓	✓
26		SIR data receiving error						✓
27		Hibernate current error					✓	✓
28		DMA reversal data error					✓	✓
29		DMA address error					✓	✓

Bug No.		Outline	R1.0	R1.1	R1.2	R1.3	R1.4	R2.0
30		RTC Long specification change					✓	✓
31		Audio output error						✓
32		HSP register access error						Note 3
33		Pen status hold error						✓
34		PIU touch interrupt error						✓
35		PIU touch pressure detection error						✓
36		GPIO interrupt startup specification change						✓
37		GPIO interrupt error						✓
38		DCD interrupt error					Note 3	Note 3
39		TClock timer error						✓
40		LED register value error						✓
41		Address error						✓
42		Restrictions on RTC counter value read					Note 3	Note 3
43		RTC register write error						✓
44		Restriction of key Auto Scan						Note 3
45		RTC reset restriction						Note 3

Bug No.		Outline	R1.0	R1.1	R1.2	R1.3	R1.4	R2.0
47		A/D error	💣	💣	💣	💣	✋	✓
48		DSIU communication transfer rate error	💣	💣	💣	💣	✋	✓
49		FIR bug	💣	💣	💣	💣	💣	✋
50		GPIO output enable bug	💣	💣	💣	💣	💣	✋

NOTES:
1. Correction for the AUDIO send/receive DMA only.
2. Some restrictions remain.
3. This will be included in the next version of the specification i. e. shall be regarded as part of the specification.

✓: No problem

✋: Bug (will be corrected by next version upgrade)

💣: Bug (restriction, not corrected by version upgrade)

(B) BUG DESCRIPTION

Bug No.	Outline	Description
1	Sizing is not performed in the high-speed system bus memory space.	[Description] Sizing is not performed in the high-speed system bus memory space. [Countermeasure until correction] **Do not perform bus sizing form the ISA high-speed system bus memory space.**
2	When different values are assigned to WLCD/M[2:0] and WISAA[2:0], read access is not possible and hangup occurs.	[Description] When different values are assigned to WLCD/M[2:0] and WISAA[2:0], read access is not possible and hangup occurs. [Countermeasure until correction] **When using the ISA high-speed system bus memory space, assign the same value to WLCD/M[2:0] and WISAA[2:0] of BCUSPEEDREG(0x0b000000a).**
3	It is not possible to set bit 16 of the physical address of the DMA buffer to "1" for audio input.	[Description] It is not possible to set bit 16 of the physical address of the DMA buffer to "1" for audio input, so the following unsettable spaces occur in the audio input DMA addresses. [Examples of physical DMA buffer address for audio input] 0x0005FFFF to 0x00050000 Unsettable 0x0004FFFF to 0x00040000 Settable 0x0003FFFF to 0x00030000 Unsettable 0x0002FFFF to 0x00020000 Settable 0x0001FFFF to 0x00010000 Unsettable 0x0000FFFF to 0x00000000 Settable [Countermeasure until correction] Do not set addresses 0x0005FFFF to 0x00050000, 0x0003FFFF to 0x00030000 or 0x0001FFFF to 0x00010000 as DMA buffer addresses for audio input. **NOTE: Because of the DMA error described in error no. 16, it is not possible to perform DMA transfer for addresses other than the above as well.**
4	It is not possible to read from DRAM in the 16-bit bus mode.	[Description] It is not possible to read from DRAM in the 16-bit data bus mode. [Countermeasure until correction] Use the 32-bit data bus mode.
5	An overrun occurs in the CPU core while the bus is being held.	[Description] The CPU overruns because it is not possible to stop the bus access requests from the CPU core while the bus is being held. [Countermeasure until correction] Do not use the bus hold function. (Do not assert the BUSHLD* pin.) [Restrictions for Rev. 1.1 and 1.2 according to these corrections] The pre-charge specifications for the DRAM are as follows: Prior specifications / Rev 1.1 / 1.2 After normal access / min 2T Clock / min 1T Clock After self refresh / min 4T Clock / min 1T Clock

6	Depending on the access size, it may not be possible to access SIU, FIR or HSP.	[Description] Depending on the access size, it may not be possible to normally access SIU, FIR or HSP. [Countermeasure until correction] Use only the following access sizes when accessing SIU, FIR and HSP. SIU: 1-byte access FIR: 1-byte access HSP: 1-byte access (When "1" is set for the HSP BYTE bit) 1- or 2-byte access (When "0" is set for the HSP BYTE bit)
7	Deadlock may occur during block read from the PageROM.	[Description] Deadlock occurs during block read from the PageROM. [Countermeasure until correction] Do not use PageROM access. (Set "0" in PageROM0 bit and PageROM2 bit of BCUCNTREG1 (0x0b000000).) [Restrictions for Rev. 1.1 and 1.2 according to these corrections] 1. Set the access size for PageROM to the following values: Set "1" for the PAGE128 bit of the BCUCNTREG1 register. Set 01 or 00 for the WPROM bit (bit[13:12] of the BCUSPEEDREG register. 2. A bus time out cannot be detected while the bus is held, so clear the BUSHERREN bit of BCUCNTREG1 to "0".
8	During SIR communication, the IRDOUT signal is fixed at low level.	[Description] During IrDA-SIR communication, the IRDOUT signal is fixed to Low level. [Countermeasure until correction] Do not use SIR communication.
9	It is not possible to read the value assigned to the output data by GPIO.	[Description] If GPIO[31:0] is set to output, the value assigned as output data cannot be read. [Countermeasure until correction] If GPIO[31:0] is set to output, save the value assigned to the GIUPIODL/H register in memory, and use it the next time when setting output data and perform Read modified Write.
10	TPX[1:0] does not become High immediately after RTCRST.	[Description] After RTCRST, the status of the the TPX[1:0] pin does not become High, so it is not possible to detect when the touch panel is pressed immediately after RTCRST. [Countermeasure until correction] After RTCRST, do not try to detect when the touch panel is pressed until PIU is reset.

11	The pen-touch interrupt logic is Low active.	[Description] The pen touch interrupt logic is Low active, so the touch detection sequencer starts in the Wait Pen Touch status even though the touch panel has not been pressed. [Countermeasure until correction] If it is possible to install a circuit that inverts the input to TPY[1] just when TPX[1] or TPX[0] are driving High, this error can be avoided. In this case, however, it is not possible to detect the touch pressure.
12	Bit 12 of PIUCMDREG cannot be written to, and when writing to bit 9, both bits 9 and 12 are written to.	[Description] It is not possible to write to the STABLEON bit (bit 12) of PIUCMDREG (0x0b00012a), and when writing to the TPXEN[1] bit (bit 9), both the STABLEON bit and TPXEN [1] bit are written to. [Countermeasure until correction] If data is to be set in the STABLEON bit (bit 12) of PIUCMDREG(0x0b00012a), set the data in the TPXEN[1] bit (bit 9) instead.
13	The voltage of pin ADIN[3:0] cannot be sensed during ADP scanning.	[Description] The voltage of the ADIN[3:0] pin cannot be sensed during ADP scanning. [Countermeasure until correction] Use CMD scanning when scanning ADIN[3:0].
14	The voltage of ADIN[3:0], TPX[1:0] and TPY[1:0] cannot be sensed during CMD scanning.	[Description] The voltage of ADIN[3:0], TPX[1:0] and TPY[1:0] cannot be sensed during CMD scanning. [Countermeasure until correction] When performing CMD scanning, set the STABLEON bit (bit 12) of PIUCMDREG (0x0b00012a) tp "1". NOTE: Until error No. 12 is corrected, set the TPXEN[1] bit (bit 9) instead of the STABLEON bit (bit 12) to "1".
15	The AUDIOOUT pin can only output Low level.	[Description] The AUDIOOUT pin status is only capable of Low-level output regardless of the output data. [Countermeasures until correction] Audio output cannot be used.
16	The CPU becomes deadlocked when DMA transfer is performed.	[Description] When performing DMA transfer, no acknowledgment is returned from the DCU so the CPU becomes deadlocked. [Countermeasures until correction] DMA (audio input/output, FIR output) cannot be used.

<table>
<tr><td>17</td><td>Even though serial receiving data is read from the SIURB register, receiving data ready may not be cleared.</td><td>[Description]
The receive data ready bit of the SIULS register is set before the serial data is completely received (not mentioned in the specifications), so if the serial data is read from the SIURB register immediately after the receive data ready bit is set, the receive data ready bit may not be cleared.
NOTE: This specification is regarded as a restriction.
[Remedy]
After the receive data ready has been set for the SIULS register, wait for the length of time equal to the bit width of the stop bit, then read the data from the SIURB register.</td></tr>
<tr><td>18</td><td>Deadlock occurs when the reading speed for the FLASH memory is set at the same time as accessing ROM.</td><td>[Description]
If either the ROMWEN0 bit or ROMWEN2 bit of the BCUCNTREG1 register (0x0b000000) is set to "1", the CPU may become hungup.
[Countermeasure until correction]
If either the ROMWEN0 bit or ROMWEN2 bit of the BCUCNTREG1 register (0x0b000000)is set to "1", make sure that neither cache access or double-word access occur. In addition, set the WROMA[2:0] bits of the BCUSPEEDREG register (0x0b00000a) to "111" or "101."</td></tr>
<tr><td>19</td><td>The QFP pin assignment is different from the specifications, and pin 55 comes at the marker position.</td><td>[Description]
The QFP pin assignment differs from the specifications, and pin no. 55 (VDD) comes at the marker position.

1: VDD 55: VDD 109: VDD 163: VDD
2:DATA[0] 56: AGnd 110: GPIO[0] 164:BATTINH/BATTINT*
: : : :
53: RSTSW* 107: GPIO[1] 161: ILCSENSE 215: JOW*
54: Gnd 108: Gnd 162: Gnd 216: Gnd

The correct and incorrect version can be distinguished by the marking on top of the package. A package marked "VR4102 ES1.0 9713i2902" or "VR4102 ES1.0 9713i2903" is incorrect.
[Countermeasure until correction]
Set the QFP marker position as pin no. 55 (VDD).</td></tr>
<tr><td>20</td><td>The RSTOUT signal does not become High during RSTSW pin assert.</td><td><u>20. RSTOUT pin error (already corrected)</u>
[Description]
The RSTOUT signal does not become High after RSTSW pin assert.
[Countermeasure until correction]
After restarting RSTSW, use the RSTOUT bit of BCUCNTREG1 (0x0b000000) and the software to create a RSTOUT signal.</td></tr>
</table>

<table>
<tr><td>21</td><td>2 bits are missing from the SDO output data.</td><td>[Description]
When the AFESEL bit of the HSPINIT register is cleared to "0" and used in the SGS and AT modes, 2 bits of the data output to the SDO pin are missing. There was a memory error of the AFESEL bit of the HSPINIT register.
[Remedy]
Correct bit D[4:3] of the HSPINIT register. (See VR4102 Specifications (Preliminary) Ver. 3, pg. 403, Table 24 2.)

[HSPINIT register bit assignment correction]
After correction Before correction
D4 OPD AFESEL1
D3 AFESEL AFESEL0

[Bit functions]
OPD: Power-down CODEC Sets the status of the OPD* pin.
1: High level
0: Low level
AFESEL: Sets timing change of the CODEC interface.
1: ST7546, STLC7546(SGS), T7525(AT)
0: TLC320C44, TLC320AC01/02(TI)</td></tr>
<tr><td>22</td><td>Communication is not possible when using the TEMIC send/receive module.</td><td>[Description]
When the IRMSEL bit of the SIUIRSEL register is set to "01" and the TEMIC send/receive module is set, the SIRDIN pin becomes a data input pin and the FIRDIN*/SEL pin becomes a data input pin even though it is supposed to be an output pin. Therefore, the TEMIC send/receive module cannot be used.
[Countermeasure until correction]
Set the Sharp or HP module as the send/receive module for IrDA communication.</td></tr>
<tr><td>23</td><td>The status value for identifying touch/release when a touch change interrupt occurs is incorrect.</td><td>[Description]
The logic of the signal used to distinguish between touch and release is inverted, and when a touch change interrupt (penchgintr) occurs, the status of the status bits (PENSTP bit and PENSTC bit of the PIUCNTREG register) which are used to distinguish between touch and release is as follows:
PENSTP 1: The previous touch-panel status was touch.
PENSTC 0: The current touch-panel status is release.
[Countermeasure until correction]
When a touch change interrupt (penchgintr) occurs, check the status of PADSTATE[2:0] of the PIUCNTREG register and determine whether the status is touch or release.
However, when the status of PADSTATE[2:0] is 010(ADPortScan), look at and determine the status of PADSTATE[2:0] after padadpintr occurs.
PADSTATE[2:0] Touch/Release
100: WaitPenTouch Release
101: DataScan Touch
110: IntervalNextScan Touch</td></tr>
</table>

24	The interrupt is held in the register even though the GPIO interrupt type is set to through.	[Description] Even though the GPIO interrupt type for the GIUINTHTSELL register (0x0b000118) and GIUINTHTSELH register (0x0b00011a) is set to through, the interrupt factors are held in the GIUINTSTATH register (0x0b00010a) and GIUINTSTATL register (0x0b00108) in the same way as when the GPIO signal interrupt is set to hold, and after the GPIO signal is deasserted, the interrupt for appropriate bit of the GIUINTSTATH register or GIUINTSTATL register continues until WIC is performed. [Countermeasure until correction] Set the GPIO interrupt type of the GIUINTHTSELL register (0x0b000118) and GIUINTHTSELH register (0x0b00011a) to "1", and use only the hold type.
25	Register access to the FIR, SIU and HSP units connected to the internal ISA may be incorrect.	[Description] If access to the registers of the FIR, SIU or HSP units, which are connected to the internal ISA, competes with DRAM access, an error will occur in accessing the registers. [Countermeasure until correction] When accessing the registers of the FIR, SIU or HSP units, do not perform DMA transfer. Also, as shown in the sample programs below, disable interrupts before accessing the registers of the FIR, SIU or HSP units, then write "0" in BCUREFCOUNTREG register (0x0b00000e) and issue a refresh cycle. Then, after reading a dummy register, access the registers of the FIR, SIU or HSP units. li r3,0xfffffffe mfco r2,C0_Config andi r2,r2,r3 mtc0 r2,C0_Config #Interrupt Disable sh zero,0xl2(rl) #Refresh start lhu r2,0xl2(rl) #Dummy read lhu/sh r3,0xXX(r8) #Internal ISA read/write #r1:0xab000000 base address of peripherals #r8:0xac000000 base address of ISA peripherals
26	Erroneous data is received when switching from receive to send during SIR transmission.	[Description] During SIR transfer, incorrect 1 data is received after switching from receive to send. [Countermeasure until correction] In SIR transfer, after switching from receive to send, clear the buffer after the data has been completely sent, or read the data and delete it.
27	During Hibernate, 500uA or more current flows.	[Description] Hibernate allows current of 500uA or more to flow. [Countermeasure until correction] None.

28	DMA transfer directly after LCD access makes DMA transfer data become reversed.	[Description] When GMODE bit is set to 0 for BCUCNTREG2 (0x0b00002) register and LCD access data is set to be reversed, DMA transfer directly after the LCD access results in the DMA transfer data also being reversed. [Countermeasure until correction] Set GMODE bit to 1 for BCUCNTREG2 register and use a mode which does not reverse LCD access data.
29	After accessing LCD of larger size than the word, or accessing external ISA, DMA transfer accesses wrong address.	[Description] After accessing an LCD of a larger size than a word, or accessing an external ISA, the lower 4 bits of DMA transfer address become wrong, that is, they becomes the ones which were used with the latest LCD access or external ISA access. [Countermeasure until correction] None.
30	RTCLong interrupt has been added as a factor in startup from Suspend mode.	[Description] RTCLong interrupt has been added as a startup factor from Suspend mode for compatibility with VR4101 [Countermeasure until correction] None.
31	Assigning 0x0 to D/A converter for audio output makes the output pin unstable.	[Description] Assigning 0x0 to the D/A converter for audio output makes the output pin unstable. [Countermeasure until correction] Do not assign 0x0 to the D/A converter. Use 0x1 instead.
32	Successively accessing HSP unit register causes access error.	[Description] Successively accessing HSP unit register causes an access error. [Countermeasure until correction] To avoid successive access to the HSP unit register, insert sufficient instructions, such as 12 or more NOP instructions, which do not execute register access.
33	An error occurs in the "penstatus" bit which indicates the pen touch or release status.	[Description] The Penstatus bit which indicates the pen touch/release status on PIU is correctly held when Penchgintr = "1", but the TPY1 pin status is made visible to the through when Penchgintr = "0". [Countermeasure until correction] When Penchgintr = "0", ignore the content of Penstatus.

<table>
<tr><td>34</td><td>A touch interruption occurs whenever the touch panel’s sequencer state changes from "standby" to "WaitPenTouch".</td><td>[Description]
Whenever the touch panel’s scan sequencer state changes from "standby" to "WaitPenTouch", it takes time for the input voltage to the interrupt pin (TPY1), affected by the capacity composition of the touch panel, to move from the active level to the inactive level. This causes a touch interruption to take effect despite the fact that the touch panel is not actually touched.
[Countermeasure until correction]
When the state has moved from Standby to WaitPenTouch, ignore the initial Penchgintr and clear the cause.</td></tr>
<tr><td>35</td><td>An error occurs in the touch pressure detection value when the difference between the pull-down resistor value of the touch panel interrupt terminal and the resistor value at panel touch is excessively large.</td><td>[Description]
When the difference between the pull-down resistor value of the touch panel interrupt terminal (TPY1) and the resistor value at panel touch is excessively large, the difference between the large and small touch pressures cannot be obtained as the value difference. And, if the pull-down resistor’s value of the TPY1 pin is too large, the level stabilization period becomes longer due to the panel’s capacity composition. This causes an exposed level at ADC before the due time.
[Countermeasure until correction]
Lower the value of the interrupt pin (TPY1)’s pull-down resistor to about 10k?. (Use this resistor value 10k? as a guide. Set a value appropriate to each system by conducting an assessment.)</td></tr>
<tr><td>36</td><td>GPIO [9:12] interrupt has been added to the startup cause from the Hibernate mode.</td><td>[Description]
GPIO [9:12] interrupts are added to the return cause from the Hibernate mode. To maintain the compatibility with the conventional products, the default is set to "undetected" and the startup detection cannot be detected in the post-reset state.

PMUINT2REG(0x0b0000a4) Startup cause display:

[15] GPIO12INTR R/W1C 1: Detected; 0: Undetected default 0
[14] GPIO11INTR R/W1C 1: Detected; 0: Undetected default 0
[13] GPIO10INTR R/W1C 1: Detected; 0: Undetected default 0
[12] GPIO9INTR R/W1C 1: Detected; 0: Undetected default 0
[11:0] Reserved R --- default 0

PMUCNT2REG(0x0b0000a6) Startup cause mask and edge specification:

[15] GPIO12MSK R/W 1: Startup enabled; 0: Startup disabled default 0
[14] GPIO11MSK R/W 1: Startup enabled; 0: Startup disabled default 0
[13] GPIO10MSK R/W 1: Startup enabled; 0: Startup disabled default 0
[12] GPIO9MSK R/W 1: Startup enabled; 0: Startup disabled default 0
[11] GPIO12TRG R/W 1: 1: Falling edge; 0: Rising edge default 0
[10] GPIO11TRG R/W 1: 1: Falling edge; 0: Rising edge default 0
[9] GPIO10TRG R/W 1: 1: Falling edge; 0: Rising edge default 0
[8] GPIO9TRG R/W 1: 1: Falling edge; 0: Rising edge default 0
[7:0] Reserved R --- default 0</td></tr>
</table>

37	The GPIO [15:9] and GPIO (3:00) interrupts cannot achieve a return from the Suspend mode.	[Description] Because the interrupts from the edge trigger type GPIO [15](DCD), GPIO[14:9] (Mclk synchronous interrupt) and GPIO[3:00](RTC synchronous interrupt) cannot be accepted in Suspend mode, it is not possible to use these interrupts to perform the return from the Suspend mode. [Countermeasure until correction] When using GPIO[15:9] and GPIO[3:0] as return interrupts from the Suspend mode, clear the relevant bits of the GIUINTTYPL (0x0b000110) and GIUINTTYPH (0x0b000112) registers to 0 and set the interrupt type to the level trigger. Or, use "38. DCD interrupt error" NOTE to achieve a startup by means of the DCD interrupt via SIU.
38	Gets started up with the DCD interrupt (SIU) from the Suspend mode.	[Description] When in Suspend mode, the change interrupt of the DCD signal via SIU causes a return from the Suspend mode. **NOTE: This shall be regarded as a specification.** [Remedy] Before entering the Suspend mode, clear the MSKSSIU bit (bit8) of the CMUCLKMSK register (0x0b000060) to 0 and then mask the clock supply of 18.432MHz.
39	Writing the TClock timer setup in half words may result in entering an incorrect value into the counter.	[Description] In essence, when values are written into both the TCLKHREG(0x0b0 0lc2) register and the TCLKLREG(0x0b00 0lc0) register, which set the Tclk counter cycle of the RTC unit, these values are reflected in the TCLKCNTHREG(0x0b0 01c6) and TCLKCNTLREG(0x0b0 01c4) registers, which are Tclk counters, to start the countdown. However, with this error, if the Tclk counter becomes 0x000 00001, the data at that time will be reflected as the counter values in the TCLKCNTHREG and TCLKCNTLREG registers and the countdown will be performed, even before values are written into the TCLKHREG and TCLKLREG registers. [Countermeasure until correction] When writing into TCLKHREG and TCLKLREG, make sure to write data in terms of words; or, when writing into TCLKHREG and TCLKLREG, mask the TCLK counter interrupt to prevent any illegal TClock interrupt from occurring even when an illegal value has been assigned temporarily.
40	After RTC resetting, the LED unit's register values become illegal.	[Description] After RTC resetting, the initial values are not assigned to the registers (LEDHTSREG, LEDLTSREG, LEDCNTREG, LEDASTCREG) of the LED unit, so these registers remain undetermined. [Countermeasure until correction] After RTC resetting, set the following values for the LED registers. *LEDHTSREG(0x0b00 0240)0x0010 *LEDLTSREG(0x0b00 0242) : 0x0020 *LEDCNTREG(0x0b00 0248)0x0002 *LEDASTCREG(0x0b00 024a) 0x04B0

41	When an address error exception occurs, the value may not be stored in the BadV Addr register.	[Description] When an instruction address error exception has occurred simultaneously with the following stall, the virtual address is not stored in the Badvaddr register. Stall causes include the cache instruction which comes three instructions before the address-errored instruction, an immediately preceding cache error, or a uTLB error from the immediately preceding instruction. (refer to table below) [Countermeasure until correction] An address error caused by the instruction fetch can be avoided by referring to the EPC register instead of the BadVAddr register. No remedy is available for address errors that have been caused by a data access.
42		
43	When reading the RTC's counter value, the reading must be done twice.	[Description] Depending on the reading timing, it may not be possible to correctly read ETIMELREG(0x0b0000c0), ETIMEMREG(0x0b0000c2), ETIMETHREG(0x0b0000c4), RTCL1CNTLREG(0x0b0000d4), RTCL1CNTHREG(0x0b0000d6), RTCL2CNTLREG(0x0b0000dc) and RTCL2CNTHREG(0x0b0000de). **NOTE: This specification shall be regarded as a restriction.** [Remedy] When reading the RTC register above, use the values that have been read by the following procedure. 1. Read the same register twice. 2. If the results that have been read are the same, use this value. 3. If the results that have been read are not the same, read the register again and compare the result with the previous ones. 4. Repeat steps 2 and 3 above until the resulting values match each other. This phenomenon shall be regarded as a specification.

44	Writing to the RTC register may not be performed correctly.	[Description] Depending on the reading timing, it may not be possible to correctly read ETIMELREG(0x0b0000c0), ETIMEMREG(0x0b0000c2), ETIMEHREG(0x0b0000c4), ECMPLREG(0x0b0000c8), ECMPMREG(0x0b0000ca), ECMPHREG(0x0b0000cc), RTCL1LREG(0x0b0000d0), RTCL1HREG(0x0b0000d2), RTCL2LREG(0x0b0000d8) and RTCL2HREG(0x0b0000da). [Remedy] Write the RTC register above according to the following procedure. 1. Disable all the interrupts. 2. Read ETIMELREG(0x0b0000c0) twice. 3. If the results that have been read are not the same, write the values into the target register. 4. If the results that have been read are the same, perform the register reading once more on the ETIMRLREG(0x0b0000c0) and compare the value with the previous ones. 5. Repeat steps 2 and 3 above until the resulting values don't match each other. The reason you must check that the values resulting from reading the ETIMELREG twice in the sequence above do not match each other, is to detect the rising edge of the 32kHz clock.
45	The scanning sequence may suddenly end in the middle of automatic key scanning.	[Description] In the event that the keyboard interface has been set for automatic key scanning, the system may automatically return to the wait key scan state after a key scanning sequence is executed upon detection of a key entry. **Caution: This specification shall be regarded as part of the restriction.** [Cause] Despite the fact that the key sequencer is in the "Stopped" state (displayed in the KIUSCANS register (0x0b000192)), setting the SCANSTP bit (bit3) of the KIUSCANREP register (0x0b000190), which instructs the key scanning to stop, does not clear the SCANSTP bit because the sequencer has already stopped. This is because if the sequencer subsequently starts operation, an attempt is made to stop this sequence. A supplementary explanation of the SCANSTP bit specification is provided here. A corrective action to take when this phenomenon has occurred by setting the SCANSTP bit while the key sequencer is in the "Stopped" state is also described below. [Specification] Setting the SCANSTP bit (bit3) of the KIUSCANREP register (0x0b000190) to 1 results in clearing this bit to 0 after forcibly stopping key scanning. However, the operation varies depending on the key sequencer condition at the time the SCANSTP bit is set. Stopped: Setting the SCANSTP bit when it is in the Stopped state puts SCANSTP in hold (with the SCANSTP bit remaining set to 1) because no scanning operation to be stopped is available. Thus, by the time the next key scanning is executed once, the key scanning is forcibly

		stopped and the SCANSTP bit is cleared to 0. (Stopped -> WaitKeyIn -> Scanning -> Stopped) WaitKeyIn: Setting the SCANSTP bit when it is in the WaitKeyIn state puts SCANSTP in hold (with the SCANSTP bit remaining set to 1) because no scanning operation to be stopped is available. Thus, once the key scanning which has started is executed, the key scanning is forcibly stopped and the SCANSTP bit is cleared to 0. (WaitKeyIn -> Scanning -> Stopped) Scanning: Setting the SCANSTP bit when it is in the Scanning state forcibly stops the key scanning after the current scanning is ended, without moving on to the next scanning, and clears the SCANSTP bit to 0. (Scanning -> Stopped) IntervalNextScan: Setting the SCANSTP bit when it is in the IntervalNextScan state stops the key scanning and clears the SCANSTP bit to 0 immediately. (IntervalNextScan -> Stopped) Key Sequencer State Transition Diagram [Countermeasure] If Key Auto Scan has been set and the SCANSTP bit also has been set regardless of the sequence state, use the software to check whether the key scanning sequence has been completed each time a key scan sequence is executed. (ex. if key data is 0 and there is no data, another key scan sequence is required.) When another key scan sequence is required, set SCANSTART bit (bit2) of the KIUSCANREP register (0x0b000190) to 1 to forcibly start an another key scan sequence.
46	Until the 32k clock starts oscillation after power ON, the processor's pin status remains undefined.	[Description] From the time RTCRST is asserted until the 32k clock starts oscillation after power ON, the processor's pin status remains undefined. After the 32k clock oscillation is started, the processor pin status is defined as the status at the time of RTCRST in the specification. **Caution: This specification shall be regarded as part of the specification.** [Cause] This is caused by the fact that an undefined state is created in the CPU with the reset not taking effect from when the power is turned on till the 32k clock starts oscillation, because the reset signal inside the CPU is operating synchronously with the 32k clock. [Countermeasure] No countermeasure is available. However, because RTCRST is always input to the CPU after the power is turned on and after the period of the undefined status, this phenomenon will not affect the CPU.
47	Performing an audio recording while operating a touch panel or using a general-purpose A/D port results in	[Description] Entering audio input with AIU when performing A/D conversions such as touch panel operation and battery pressure measurement, etc. may result in entering incorrect data. This error is a phenomenon which occurs only to AIU when the PIU or general-purpose A/D input and the AIU attempt to use the A/D converter simultaneously thus causing a

	recording invalid data.	conflict. [Countermeasure until correction] Do not use the touch panel and the general-purpose A/D port during audio input.
48	The DSIU communications are performed at a speed different from the baud rate that has been set.	[Description] The DSIU communication is performed at a speed different from the baud rate that has been set with the BPRO[2:0] bit of the BPRMOREG register (0x0b00 01h6). The ratio of the communication transfer rate error varies depending on the CLKSEL[2:0] status (i.e. the internal operating frequency of the CPU core) as shown below. CLKSEL = 111 Baud rate of about 200% of original set value CLKSEL = 110 Baud rate of about 159% of original set value CLKSEL = 101 Baud rate of about 133% of original set value CLKSEL = 100 Baud rate of about 109% of original set value CLKSEL = 011 Baud rate of about 93% of original set value CLKSEL = 010 Baud rate of about 79% of original set value CLKSEL = 001 Baud rate of about 63% of original set value CLKSEL = 000 Baud rate of about 50% of original set value [Countermeasure until correction] No countermeasure is available.
49	Due to its unsatisfactory clock generation, the FIR unit does not function.	[Description] Due to a clock generation bug, the FIR unit does not function. [Countermeasure until correction] No countermeasure is available.
50	When in 16bit bus mode, the GPIO[26:29]'s output enable does not function.	[Description] When in 16bit bus mode, setting the IOS[13:10] of the GIUIOSELH register (0x0h00 0102) to 1 results in setting the corresponding GPIO(GPIO[29:26]) for the output. However, only a low level is output regardless of the PIOD[13:10] setting of the GIUPIODH register (0x0h000106). [Cause] Because not the GIUIOSELH register IOS[13:10] but IOS[15] (the selection condition bit of the GPIO[34]'s output value) is mistakenly used as the condition for selecting the GPIO[29:26]'s output value. [Countermeasure until correction] When using the GPIO[29:26] as an output pin, make sure that both GPIO [29:26] and GPIO[31] are used as output pins. Specifically, always set the GIUIOSELH register IOS[15] and IOS[13:10] to the same value.

Illustrating table Bug # 41:

Pipeline operation

RF	EX	DC (cache instruction)	WB	
IF	RF	EX	DC	WB
	IF	RF	EX	DC
		IF (Address error)	RF	EX

Or,

IF	RF	EX	DC	WB
	IF	RF (Cache error / uTLB error)	EX	DC
		IF (Address error)	RF	EX