Concerned Products:	**Customer Notification**	Date: August 27th 2001
		NEC-Electronics (Europe) GmbH EAD -Technical Product Support
IE-703089-MC-EM1	**Bug Report**	Source Doc: NEC Tokyo SUD-T-5220-2-E
		Author: T.Kreye

History	Date	Doc. No.
1st issue	August 27th 2001	TPS-HE-B-2780

(A) BUG/RESTRICTION LIST

Bug No.	Outline	IE-703089-MC-EM1		
	Rev.	V1.00	V1.10	V1.11
	Control Code	A	B	C
1	4.2 V target supply voltage restriction	💣	✓	✓
2	Emulation probe restriction	💣	✓	✓
3	Restriction on reading registers of CSI5/6	💣	💣	✓
4	Cascading timer 0 and timer 6 not possible	💣	💣	✓

Note: Please see also section C “Additional Cautions”

✓: No problem
✋: Bug (will be corrected by version upgrade)
💣: Bug (not planned to be corrected by next version upgrade)

(B) DESCRIPTIONS OF BUGS / USAGE RESTRICTIONS

No.	Outline	Description
1	4.2 V target supply voltage restriction	*Details* Emulation cannot be performed if the target power supply voltage (VDD0, VDD1) is below 4.2 V. This bug has been corrected in control code B and later products. *Workaround* When target board is connected, use a power supply voltage (VDD0, VDD1) of at least 4.2 V.

No.	Outline	Description
2	Emulation probe restriction	*Details* Drills are missing in the emulation probe socket to allow a connection with a socket using “YQ-Guide” pins or the “SWEX-144SD” emulation probe adapter. This bug has been corrected in control code B and later products. *Workaround* - Remove “YQ-Guide” pins before connecting to emulation board socket. or - Use “YQ-Socket” as height adapter between socket using “YQ-Guide” pins and emulation board socket.

No.	Outline	Description
3	Restriction on reading registers of CSI5/6	*Details* Reading of I/O register values related to 3-wire serial I/O channel 5 & 6 is impossible with CPU clock (f_{CPU}) greater than 10 MHz. Note: I/O registers can be written as usual even when f_{CPU} is operating at more than 10 MHz. This bug has been corrected in control code C and later products. *Workaround* Set f_{CPU} to 10 MHz or less when reading I/O registers of CSI5/6.

No.	Outline	Description
4	Cascading timer 0 and timer 6 not possible	*Details* Timer 0 overflow signal cannot be selected using timer clock selection register of timer 6. If the timer clock selection of timer 6 is set to “TM0 overflow signal” (TCL60=0x07, TCL61=0x01), the timer clock will set to fxx/256. The TM0 overflow signal cannot be selected. This bug has been corrected in control code C and later products. *Workaround* None

(C) ADDITIONAL CAUTIONS

No.	Outline	Description
1	Voltage supply	Satisfy the following conditions when using the IE-703089-MC-EM1 with other than VDD0 = VDD1 = ADCVDD = PORTVDD0 = PORTVDD1 = POERTVDD2. a) PORTVDD1<=PORTVDD2 when using FCAN controller. b) VDD0 = ADCVDD = 4.5 V to 5.5 V when using the A/D converter.

(D) Revision History

Initial issue:

Author: T.Kreye

- Date: August 27th 2001