

## Customer Notification

# QB-78K0RFX3

## In-Circuit Emulator

## Operating Precautions

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### Target Devices

**78K0R/FB3 Series**

**78K0R/FC3 Series**

**78K0R/FE3 Series**

**78K0R/FF3 Series**

**78K0R/FG3 Series**

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## A) Table of Operating Precautions for QB-78K0RFX3

Table A-1 Summary of restrictions

No.	Outline	Control Code <sup>Note</sup>	QB-78K0RFX3				
			A	B	C	D	E
1	Self-programming support (Technical Limitation)		×	×	✓	✓	✓
2	Data Flash support (Technical Limitation)		×	×	○	○	○
3	AD Converter (Technical Limitation)		×	×	✓	✓	✓
4	Dead lock condition (Technical Limitation)		×	✓	✓	✓	✓
5	EEPROM emulation in Code Flash (Direction of use)		×	×	×	×	×
6	Trace data when an interrupt occurs (Technical Limitation)		×	×	×	✓	✓
7	IIC: Acknowledge error bit is set erroneous (Technical Limitation)		×	×	×	×	✓

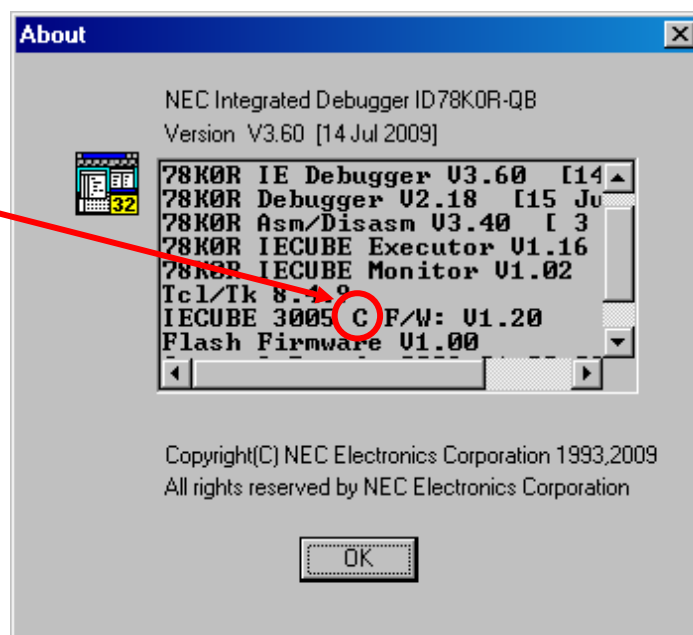
✓: Not applicable

×: Applicable

○: Please refer to details in the description part

### Note:

- The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.
- The control code can be checked by selecting [About] from the [Help] menu when the ID78K0R-QB is running. "X" in version information "IECUBE \*\*\*\* X F/W \*\*.\*\*\*" is the control code.



## B) Description of Operating Precautions for QB-78K0RFX3

Table B-1 No. 1 Self-programming support (Technical Limitation)

<p><u>Details</u> Self-programming is not supported.</p> <p><u>Workaround</u> Will be corrected in the version up.</p>
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Table B-2 No. 2 Data Flash support (Technical Limitation)

<p><u>Details</u> Data Flash is not supported due to missing EEPROM Emulation Library</p> <p><u>Workaround</u> Will be corrected in the version up.</p> <p><b>Note:</b> For QB-78K0RFX3 with Control Code "C" and later the access to the Data Flash area is supported (i.e. write, erase block, blank check, read, ...), although the EEPROM Emulation and Data Flash Access library are still under development.</p>
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Table B-3 No. 3 AD Converter (Technical Limitation)

<p><u>Details</u> The following issues exists on the AD Converter: a) When the conversion time is short in SCAN mode the switching noise for the analog input selector will cause an inaccurate ADC result. b) Due to some high capacitance on the I/O Board, the ADC accuracy might become worse in High-Speed conversion mode</p> <p><u>Workaround</u> Will be corrected in the version up.</p>
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Table B-4 No. 4 Dead lock condition (Technical Limitation)

<p><u>Details</u> The CPU will went in a Dead lock when the following condition is met: When the STOP instruction is executed direct after clearing PLLON the CPU will enter in a dead lock.</p> <p><u>Workaround</u> Will be corrected in the version up.</p>
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Table B-5 No. 5 EEPROM emulation in Code Flash (Direction of use)

Details

While performing EEPROM emulation in the Code Flash and using one of the following error emulation settings: 'EEPROM\_Write Error(Verify)' or 'FlashBlockVerify Error(verify)' In case an error occurs, both errors will be generated.

Table B-6 No. 6 Trace data when an interrupt occurs (Technical Limitation)

Details

If interrupt request occurs by the specific condition, the trace result may not be correct, **however the instructions itself are executed correctly**. Detailed condition and phenomenon about the trace function/display are explained below.

Condition

When branching to interrupt vector just after executing one of the following instructions, the trace display result may not be correct.

1. MOVW SP, #word
2. MOVW SP, AX
3. ADDW SP, #byte
4. SUBW SP, #byte

The above condition is relevant by the following case.

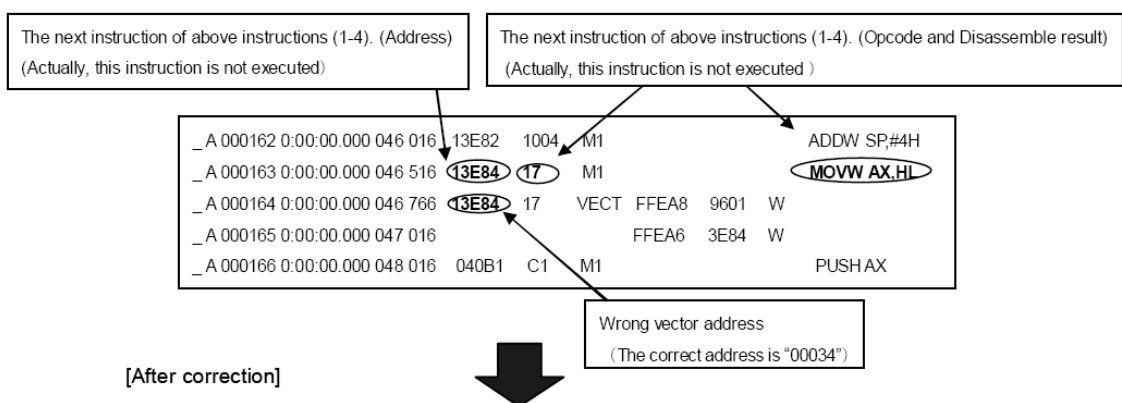
- In case of fetching ROM, 1, 2, 3 and 4 of the above instructions
- In case of fetching RAM, 3 and 4 of the above instructions

Phenomenon

When branching to interrupt vector just after executing the above instructions (1-4), the next instruction of above instructions (1-4) is not executed, thus it is not displayed on trace window. But the following contents are displayed on trace window actually.

- The next instruction of above instructions (1-4)
- The wrong vector address

[Before correction]



_A 000162 0:00:00.000 046 016	13E82	1004	M1		ADDW SP,#4H
_A 000163 0:00:00.000 046 516				FFEA8 9601 W	
_A 000164 0:00:00.000 046 766	00034	B1	VECT	FFEA6 3E84 W	
_A 000165 0:00:00.000 047 766	040B1	C1	M1		PUSHAX
_A 000166 0:00:00.000 048 016	040B2	C7	M1	FFEA4 1000 W	PUSH HL

Right vector address.

**Table B-7 No. 7 IIC: Acknowledge error bit is set erroneous (Technical Limitation)**

**General**

During IIC – bus transfer, after 8 data bits, an acknowledge is given back from the receiver when the transfer has been accepted. During the 9 th clock period, the transmitter sets high level at the data line and the receiver has to pull down the data line to low level. This is recognized in the transmitter. If there was no acknowledge, an error flag is set.

**Details**

During IIC transfer, acknowledge error flag (SSR11.PEFmn = 1) is set despite the receiver has generated an acknowledge correctly.

This behaviour is in the emulator only. In the real device, functionality is as expected.

**Workaround**

Ignore the PEF - flag error message when you use the emulator. Finally check the correct PEF - flag error message handling using the real chip.

This issue can be corrected by an update of QB-78K0RFX3 with control code D to control code E using the IECUBE upgrade tool qb-78k0rfx3\_e\_dl.exe.

This issue is corrected in the QB-78K0RFX3 with control code E.

**C) Valid Specification**

Item	Date published	Document No.	Document Title
1	August 2009 or later	ZUD-CD-09-0139 or later	Preliminary User's Manual

**D) Revision History**

Item	Date published	Document No.	Comment
1	February 9, 2009	U19675EE1V0IF00	1 <sup>st</sup> Release
2	September 21, 2009	U19675EE2V0IF00	1 <sup>st</sup> update (2 <sup>nd</sup> edition) - Corrections of description for item 1, 2 and 3 - Addition of item 4 and 5 - Addition of Control Code B and C
3	March 29, 2010	U19675EE3V0IF00	2 <sup>nd</sup> update (3 <sup>rd</sup> edition) - Addition of item 6 - Addition of Control Code D
4	May 10, 2011	R01TU0020ED0100	3 <sup>rd</sup> update (4 <sup>th</sup> edition) - Adaption to new document numbering
5	August 9, 2011	R01TU0020ED0200	4 <sup>th</sup> update (5 <sup>th</sup> edition) - Addition of item 7
6	October 11, 2011	R01TU0020ED0300	5 <sup>th</sup> update (6 <sup>th</sup> edition) - Addition of Control Code E

