NEC

Customer Notification

IE-703089-MC-EM1

In-circuit Emulator Option Board

Operating Precautions

Target Device

V850/SC1

V850/SC2

V850/SC3

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(A) Table of Operating Precautions

No.	Outline		IE-703089-MC-EM1				
		Rev.	V1.00	V1.10	V1.11	V1.22	V1.23
		Control Code	A	B	C	D	E
1	4.2 V target supply voltage restriction (Direction for use)		✗	✓	✓	✓	✓
2	Emulation probe connection (Direction for use)		✗	✓	✓	✓	✓
3	Reading registers of CSI5 / CSI6 (Direction for use)		✗	✗	✓	✓	✓
4	Timer 6 clock selection (Direction for use)		✗	✗	✓	✓	✓
5	Port 00 I/O (Direction for use)		✗	✗	✗	✓	✓
6	Access to external expansion area (Direction for use)		✗	✗	✗	✓	✓
7	FCAN: Message search (Specification change notice)		✗	✗	✗	✓	✓
8	Addition to IIC bus function (Specification change notice)		✓	✓	✓	✗	✗
9	Addition to watch timer function (Specification change notice)		✓	✓	✓	✗	✗
10	Emulation of ROM correction (Specification change notice)		✗	✗	✗	✗	✗
11	Emulation during OST after Reset (Specification change notice)		✗	✗	✗	✗	✗
12	Interrupts in IDLE / STOP mode (Direction for use)		✗	✗	✗	✗	✓
13	Hi-Z output of clockout pin (Specification change notice)		✗	✗	✗	✗	✗
14	FCAN: Time Stamp (Specification change notice)		✓	✓	✓	✗	✗
15	FCAN Main Clock Select (Direction for use)		✗	✗	✗	✗	✗
16	Voltage supply (Direction for use)		✗	✗	✗	✗	✗
17	I/O Chip Sockets		✗	✗	✗	✗	✓
18	External Bus Interface		✗	✗	✗	✗	✗

✓ : Not applicable
✗ : applicable

(B) Description of Operating Precautions

No. 1	4.2 V target supply voltage restriction (Direction for use)
	Details Emulation cannot be performed if the target power supply voltage (VDD0, VDD1) is below 4.2 V.

No. 2	Emulation probe connection (Direction for use)
	Details Drills are missing in the emulation probe socket to allow a connection with a socket using “YQ-Guide” pins or the “SWEX-144SD” emulation probe adapter. Remove “YQ-Guide” pins before connecting to emulation board socket or use “YQ-Socket” as height adapter between socket using “YQ-Guide” pins and emulation board socket.

No. 3	Reading registers of CSI5 / CSI6 (Direction for use)
	Details Reading of I/O register values related to 3-wire serial I/O channel 5 & 6 can only be done with CPU clock (f_{CPU}) < 10 MHz. Note: I/O registers can be written as usual even at f_{CPU} > 10 MHz.

No. 4	Timer 6 clock selection (Direction for use)
	Details Timer 0 overflow signal cannot be selected using timer clock selection register of timer 6. If the timer clock selection of timer 6 is set to “TM0 overflow signal” (TCL60=0x07, TCL61=0x01), the timer clock will set to fxx/256. The TM0 overflow signal cannot be selected.

No. 5	Port 00 I/O (Direction for use)
	Details Port 00 cannot be used as an output port even if it is set as to output mode by the corresponding Port mode register. Moreover, port 00 cannot read the correct input value even if set as an input port while the NMI pin function is masked in the debugger. If port 00 is set as an input port and the NMI function is not masked in the debugger, input values are read correctly.

No. 6	Access to external expansion area (Direction for use)
	Details The external expansion area (including FCAN memory area) cannot be read or written.

No. 7	FCAN: Message search (Specification change notice)

Details

This behaviour applies to devices containing 2 FCAN (uPD70F3079Y, uPD703079Y)

When both FCAN channels are used simultaneously, the receive data may be stored in an incorrect message buffer or destroyed (case a) or erroneous data may be inadvertently transmitted (case b).

a) When both FCAN channels are being used simultaneously, the following behaviour will occur if one FCAN module (e. g. FCAN 2) starts transmitting while the other FCAN module is in the process of receiving i. e. performing the acceptance filtering immediately after the EOF of the acknowledged frame.
This behaviour occurs in two different ways, depending on the setting of the last message buffer (buffer 31):

(1) If the last message buffer (buffer 31) is set as a receive buffer:
The data received by FCAN 1 is stored in message buffer 31 instead of the message buffer it was intended to be received in. Because data is not stored in the correct buffer or the contents of message buffer 31 have been destroyed, a program malfunction may occur.

(2) If the last message buffer (buffer 31) is set as a transmit buffer:
The data received by FCAN 1 is not stored in any message buffer and is therefor lost. A total network system malfunction may occur because the expected data is not received.

The behaviour described above occurs when both of the following conditions are met:

- Both FCAN channels are used simultaneously
- Mask 2 (M_CONFn.MT = 4) or mask 3 (M_CONFn.MT = 5) is set for the FCAN 1 message buffer, or when FCAN 1 receives a message with an incorrect identifier, even if mask 2 or mask 3 has not been set for the FCAN 1 message buffer.

b) When both FCAN channels are being used simultaneously, if one FCAN module (FCAN 1) starts transmitting / receiving just before the other FCAN module (FCAN 2) starts transmitting, the data in the final message buffer (buffer 31) may be transmitted instead of the data that should be transmitted from FCAN 2. If the incorrect data is inadvertently transmitted in this way, a total network system error may occur.

The behaviour described above occurs when both of the following conditions are met:

- Both FCAN channels are used simultaneously
- More than two transmit requests exist for FCAN 2

No. 8	Addition to IIC bus function (Specification change notice)

Details

Two additional registers of I2C macro offers enhanced I2C functions: **IICFn**

Address locations:

IICF0: FFFFF368H

IICF1: FFFFF36AH

IICFn

(n = 0,1)

7	6	5	4	3	2	1	0
STCFn	IICBSYn	0	0	0	0	STCENn	IICRSVn

STCFn	STTn clear flag
0	A start condition is generated
1	STTn flag is cleared.

IICRSVn	Communication reservation ON/OFF Flag
0	Communication reservation ON mode
1	Communication reservation OFF mode

STCENn	Initial start enable flag
0	After IIC operational enable (IICEn=1), the start condition cannot be generated until stop condition is detected.
1	After IIC operational enable (IICEn=1), the start condition can be generated that stop condition is not detected.

IICBSYn	I2C bus condition flag
0	Bus is released
1	Bus is busy

No. 9	Addition to watch timer function (Specification change notice)

Details

Register WTNHC (at address 0xFFFFF366) has been added. This change is related to IE-Bus and therefore only applies to V850/SC2.

No. 10	Emulation of ROM correction (Specification change notice)

Details

ROM correction cannot be emulated using IE-703089-MC-EM1

No. 11	Emulation during OST after Reset (Specification change notice)
	Details Emulation during the oscillation stabilization time (OST) after reset release cannot be performed. Emulation during the oscillation stabilization time after STOP mode release is possible.

No. 12	Interrupts in IDLE / STOP mode (Direction for use)
	Details The emulator may become deadlocked if the STOP or IDLE mode is set while the interrupt request flag for an interrupt that is not masked is set. 1.) Clear the interrupt request flag of the unmasked interrupt before setting the device to STOP or IDLE mode. If the device is inadvertently set to STOP or IDLE mode before the flag is cleared, forcibly break the program execution in the debugger and reset the emulator. 2.) If applicable do not allow to set the device to STOP or IDLE mode while the interrupt request flag for an unmasked interrupt is set.

No. 13	Hi-Z output of clockout pin (Specification change notice)
	Details The CLKOUT signal of the emulator cannot be set to high impedance state. Even if the PSC register is configured to set CLKOUT to Hi-Z output (DCLK1 = 0 and DCLK0 = 1), the same operation as 'output enable' (DCLK1 = 0 and DCLK0 = 0) is performed.

No. 14	FCAN: Time Stamp (Specification change notice)
	Details The time stamp functions issued at SOF is unavailable, means fetching timestamp at SOF for RX frames and transmit timestamp in data field for TX frames is not possible. Applying time stamps to received messages at the EOF is possible therefor fetching timestamp at EOF for RX frames can be used.

No. 15	FCAN Main Clock Select (Direction for use)

Details

The FCAN macro features a CAN Main Clock Select register (CGCS). The usage of the bit field "Memory Clock Prescaler" (MCP[3:0]) requires attention concerning a certain transition from one value to another value.
When the bit field MCP[3:0] in CGCS register has been set to "0", any further write operation to this bit field that changes the value again will result in a unexpected behavior of the FCAN macro.
The FCAN macro will not operate anymore until an external reset is applied. This caution is already given in the user's manual. This description informs about further details.

Most, if not all applications, change the value of MCP only once after the start of the program. As
after reset of the CPU the bit field MCP [3:0] is initialized to 5 these applications do not encounter
any problems and existing program codes do not have to be changed.
Applications changing the MCP-value more than once during runtime of the program need to avoid to change the MCP-value again after the MCP-value has been set to"0" or in general apply only MCP-values not equal to "0". Otherwise a H/W reset needs to be issued in order to resume communication on the FCAN macro.
Please consider two cases:

- *MCP written once after RESET*
  The application needs to avoid the critical transition from MCP = 0 to MCP = <any other value>. The application has to write the target value once after reset and afterwards this value is not changed again.
- *MCP written more than once after RESET*
  Applications that need to change the MCP-value dynamically need to perform a H/W reset when the MCP-value reads 0 and again another value (not equal 0) shall become effective. In this case follow the first case *MCP written once after RESET*.

No. 16	Voltage supply (Direction for use)

Details

Satisfy the following conditions when using the IE-703089-MC-EM1 with other than
VDD0 = VDD1 = ADCVDD = PORTVDD0 = PORTVDD1 = POERTVDD2:

1.) PORTVDD1<=PORTVDD2 when using FCAN controller.

2.) VDD0 = ADCVDD = 4.5 V to 5.5 V when using the A/D converter.

No. 17	I/O chip sockets (Specification Change Notice)

Details

In Tool versions up to control code 'D' the board is equipped with device sockets for the I/O chip.
From control code 'E' onwards, there is no socket for the I/O chip.

No. 18	External Bus Interface (Direction for use)
	Details When the external bus interface is used, the values of data lines D0 to D4 may not be read correctly.

(C) Revision History

Item	Date published	Document No.	Comments
1	16.01.2002	TPS-HE-B-2780	First release
2	17.01.2002	TPS-HE-B-2781	Added notes 5 to 16, new format
3	28.01.2002	TPS-HE-B-2782	Added control code 'E'; modified notes 8, 9; added note 17
4	26.09.2002	TPS-HE-B-2783	Added operating precaution 18 Added new disclaimer