Date: Sep. 27, 2016

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	System LSI	Document No.	TN-RIN-A011B/E	Rev.	2.00
Title	Notification of R-IN32M3 Series User's Manual Peripheral Modules (Rev.8.00 to Rev.9.00) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series User's Manual: Peripheral Modules R-IN32M3-EC, R-IN32M3-CL Rev9.00 (R18UZ0007EJ0900)	

R-IN32M3 Series User's Manual Peripheral Modules Rev. 9.00 (R18UZ0007EJ0900) has been released on Renesas website. This technical update follows revision 1.00 and includes the entirety of revised items. For details, refer to "2. Documentation Updates" given below. Please take note that items marked with "caution needed" may have severe impact on the operation of corresponding devices.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

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No	Applicable Item (Rev. 9.00 Section)	Applicable Page (Rev. 9.00)	Contents	Revised
1	2. Clocks and Resets	2-1	Complement	✓
2	2.1.1 Description of Internal Clocks	2-1	Complement	✓
3	2.1.1 Description of Internal Clocks	2-1	Complement	✓
4	2.1.2 Clock Configuration Diagram	2-2	Error correction	✓
5	2.2.2 Clock Control Registers (CLKGTD0, CLKGTD1)	2-4	Error correction	✓
6	2.3.2 (5) Reset output (RSTOUTZ output)	2-7	Error correction	✓
7	2.3.4 (1) Software Reset Register (SFTRES1)	2-10	Expression alignment	✓
8	3. CPU and Internal RAMs	3-1	Complement	✓
9	3.4.2 Read Buffer	3-3	Error correction	✓
10	3.5 Internal Data RAM	3-4	Expression alignment	✓
11	3.6 Buffer RAM	3-5	Error correction	✓
12	4. Bus Architecture	4-1	Error correction	
13	6.2 Semaphores	6-1	Error correction	✓
14	Deleted from Rev. 8.00: 6.6 Service Calls	–	Expression alignment	✓
15	7. Gigabit Ethernet MAC	7-1	Expression alignment	✓
16	7.1.1 Ethernet Interface Architecture	7-2	Expression alignment	✓
17	7.3.1 (3) Gigabit Ethernet MAC control register	7-4 ~ 7-5	Error correction	✓
18	7.3.1 (3) Gigabit Ethernet MAC control register	7-5	Expression alignment	✓
19	7.3.1 (4) Hardware function call register	7-5	Expression alignment	
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21	7.3.3.1 MDC Clock Select Register (MDCCFG)	7-7	Error correction	✓
22	7.3.4.1 MIIM Register (GMAC_MIIM)	7-9	Expression alignment	✓
23	7.3.4.1 MIIM Register (GMAC_MIIM)	7-9	Expression alignment	✓
24	7.3.4.1 MIIM Register (GMAC_MIIM)	7-9	Expression alignment	✓
25	7.3.4.1 MIIM Register (GMAC_MIIM)	7-9	Expression alignment	✓
26	7.3.4.2 TX ID Register (GMAC_TXID)	7-10	Complement	✓
27	7.3.4.3 TX Result Register (GMAC_TXRESULT)	7-10	Expression alignment	✓
28	7.3.4.3 TX Result Register (GMAC_TXRESULT)	7-10	Expression alignment	✓
29	7.3.4.4 Mode Register (GMAC_MODE)	7-11	Complement	✓
30	7.3.4.4 Mode Register (GMAC_MODE)	7-11	Complement	✓

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33	7.3.4.5 RX Mode Register (GMAC_RXMODE)	7-11	Expression alignment	✓
34	7.3.4.6 TX Mode Register (GMAC_TXMODE)	7-13	Complement	
35	7.3.4.6 TX Mode Register (GMAC_TXMODE)	7-13	Error correction	
36	7.3.4.6 TX Mode Register (GMAC_TXMODE)	7-13	Complement	
37	7.3.4.6 TX Mode Register (GMAC_TXMODE)	7-13	Complement	
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40	7.3.4.7 Reset Register (GMAC_RESET)	7-15	Expression alignment	✓
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43	7.3.4.8 Pause Packet Data Register (GMAC_PAUSEn)	7-16	Complement	✓
44	7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)	7-17	Complement	✓
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48	7.3.4.11 MAC Address Registers (GMAC_ADRnA, GMAC_ADRnB)	7-19	Expression alignment	✓
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106	10.1 Features	10-2	Error correction	✓
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119	10.2.11 Register Setup Procedure	10-17	Error correction	✓
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166	14.1 Features of TAUJ2	14-2	Complement	✓
167	14.1 Features of TAUJ2	14-2	Error correction	✓
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178	15.1 Features of WDTA	15-1	Expression alignment	✓
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180	16. Asynchronous Serial Interface J (UARTJ)	16-1	Expression alignment	✓
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201	17.1 Features of CSIH	17-2	Error correction	✓
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220	18.1 Features of IICB	18-1	Complement	✓
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255	21.9.1 Timer Input Function Selection Register (SELCNT)	21-10	Expression alignment	✓
256	21.9.1 Timer Input Function Selection Register (SELCNT)	21-11	Expression alignment	✓
257	21.9.2 Timer Trigger Source Registers (TMTFR0 to TMTFR03)	21-15	Error correction	✓
258	21.10.1 Noise Filter Setting Registers 0 to 3 (NFC0 to NFC3)	21-17	Complement	✓
259	21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)	21-21	Error correction	✓
260	21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)	21-21	Error correction	✓
261	21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)	21-22	Error correction	✓
262	21.12.2 Trigger-Synchronous Port Source Registers (RP0TFR to RP3TFR)	21-29	Error correction	✓
263	21.14 CPU Bus Operating Mode Register (CPUBUSMD)	21-31	Expression alignment	✓
264	21.15 SRAM Bridge Select Register (SRAMBRSEL)	21-32	New function	
265	22.1 JTAG interface	22-1	Error correction	✓
266	22.1 JTAG interface	22-2	Error correction	✓
267	22.1 JTAG interface	22-3	Error correction	✓
268	22.1 JTAG interface	22-3	Error correction	✓

No. 1 2. Clocks and Resets

Title of Section 2 expanded.

V8.00		V9.00	
Page	Description	Page	Description
2-1	**[2. Clocks]**	2-1	**[2. Clocks and Resets]**

No. 2 2.1.1 Description of Internal Clocks

Note3 added to CLKOUT25M0-1.

V8.00		V9.00	
Page	Description	Page	Description
2-1	**[2.1.1 Description of Internal Clocks]** CLKOUT25M0-1	2-1	**[2.1.1 Description of Internal Clocks]** CLKOUT25M0-1Note3

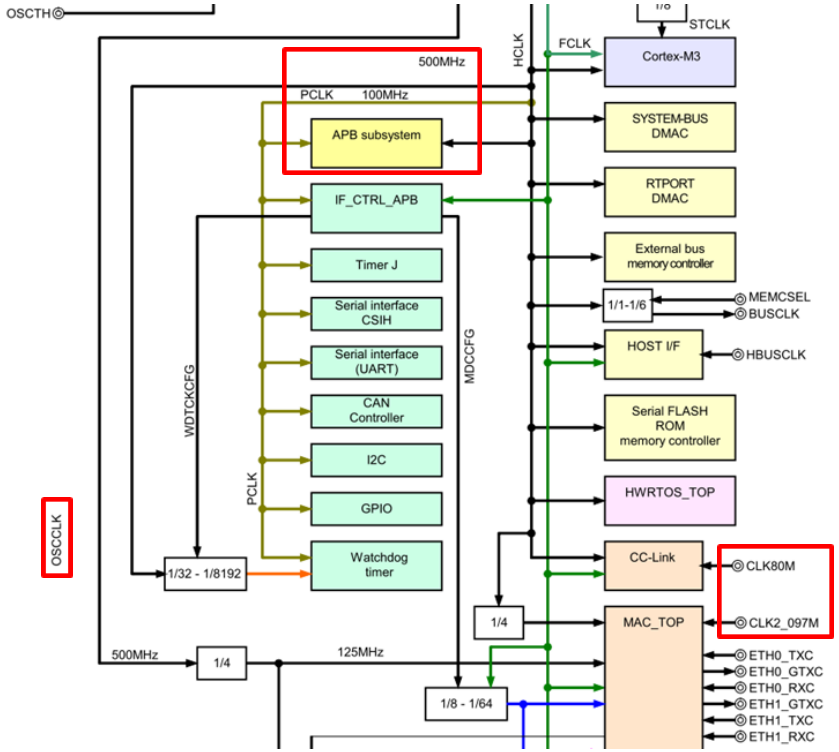
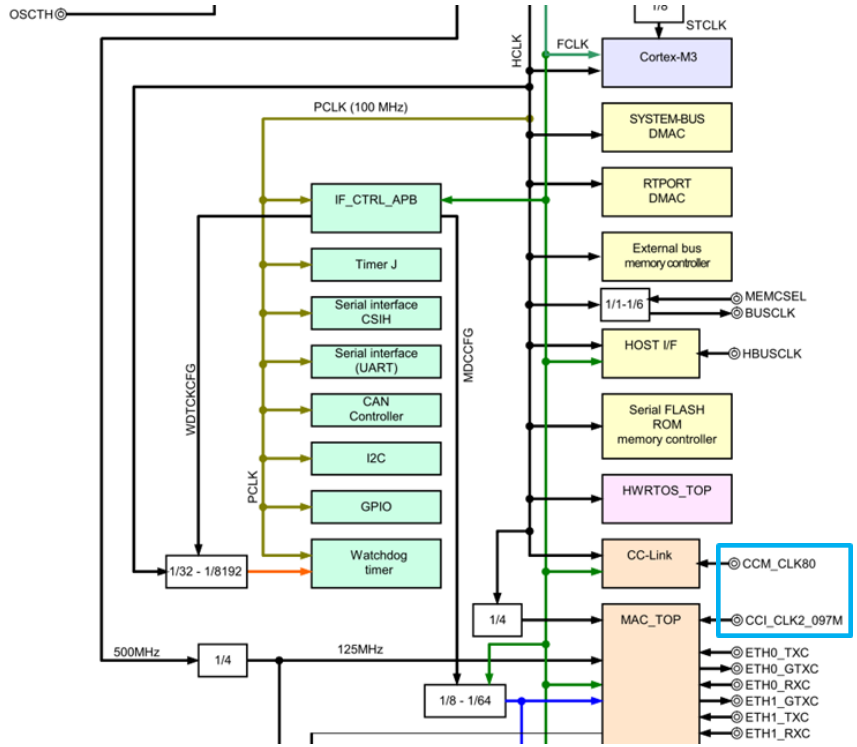
No. 3 2.1.1 Description of Internal Clocks

Note3 added.

V8.00		V9.00	
Page	Description	Page	Description
2-1	**[2.1.1 Description of Internal Clocks]** Notes 1. 2.	2-1	**[2.1.1 Description of Internal Clocks]** Notes 1. 2. 3. The CLKOUT25M0-1 pins are only provided in the R-IN32M3-CL.

No. 4 2.1.2 Clock Configuration Diagram

APB subsystem block deleted. Labels corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>2-2</td><td>[2.1.2 Clock Configuration Diagram]
[Figure 2.1 Clock Configuration Diagram]
 
</td><td>2-2</td><td>[2.1.2 Clock Configuration Diagram]
[Figure 2.1 Clock Configuration Diagram]
 
</td></tr>
</table>

No. 5 2.2.2 Clock Control Registers (CLKGTD0, CLKGTD1)

Name of Bit 13 corrected.

V8.00		V9.00	
Page	Description	Page	Description
2-4	**[2.2.2 Clock Control Registers (CLKGTD0, CLKGTD1)]** - Bit field: Bit 13 = GC2C0 [Bit Position 13: GC2C0] I2C bus (I2C0) (1: Operating, 0: Stopped)	2-4	**[2.2.2 Clock Control Registers (CLKGTD0, CLKGTD1)]** - Bit field: Bit 13 = GCI2C0 [Bit Position 13: GCI2C0] I2C bus (I2C0) (1: Operating, 0: Stopped)

No. 6 2.3.2 (5) Reset output (RSTOUTZ output)

EtherCAT reset source corrected.

V8.00		V9.00	
Page	Description	Page	Description
2-7	**[2.3.2 (5) Reset output (RSTOUTZ output)]** [Table 2.1 Reset Source and Targets to be Reset]	2-7	**[2.3.2 (5) Reset output (RSTOUTZ output)]** [Table 2.1 Reset Source and Targets to be Reset]

Table 2.1 Reset Source and Targets to be Reset (V8.00)

Reset Source	Target to be Reset: Instruction RAM Data RAM Buffer RAM	PLL	CC-Link IE Field Network Note 1 Power on reset	CC-Link	EtherCAT Note 2	CPU's debugging unit	Other peripheral circuits
PONRZ pin	✓	✓	✓	✓	✓	-	✓
RESETZ pin	-	✓	✓	✓	✓	-	✓
HOTRESETZ pin Note 1	-	-	-	✓	✓	-	✓

Table 2.1 Reset Source and Targets to be Reset (V9.00)

Reset Source	Target to be Reset: Instruction RAM Data RAM Buffer RAM	PLL	CC-Link IE Field Network Note1 Power on reset	CC-Link	EtherCAT Note2	CPU's debugging unit	Other peripheral circuits
PONRZ pin	✓	✓	✓	✓	✓	—	✓
RESETZ pin	—	✓	✓	✓	✓	—	✓
HOTRESETZ pin Note1	—	—	—	✓	—	—	✓

No. 7 2.3.4 (1) Software Reset Register (SFTRES1)

Description of RSWDT corrected.

V8.00		V9.00	
Page	Description	Page	Description
2-10	**[2.3.4 (1) Software Reset Register (SFTRES1)]** [Bit Position 4: RSWDT] Watchdog timer reset	2-10	**[2.3.4 (1) Software Reset Register (SFTRES1)]** [Bit Position 4: RSWDT] Software reset for watchdog timer

No. 8 3. CPU and Internal RAMs

Title of Section 3 expanded. introductory description modified.

V8.00		V9.00	
Page	Description	Page	Description
3-1	**[3. CPU]** This section explains information specific to R-IN32M3 products.	3-1	**[3. CPU and Internal RAMs]** This section describes an overview of the CPU and internal RAMs of an R-IN32M3.

No. 9 3.4.2 Read Buffer

Description of Read Buffer corrected.

V8.00		V9.00	
Page	Description	Page	Description
3-4	**[3.4.2 Read Buffer]** A 2-bit ECC error at the time of the read response is handled as an error in response to the AHB, and an ECC error interrupt is generated.	3-3	**[3.4.2 Read Buffer]** A 2-bit ECC error at the time of the read response is handled as an ECC error interrupt is generated.

No. 10 3.5 Internal Data RAM

Description of Internal Data RAM modified.

V8.00		V9.00	
Page	Description	Page	Description
3-5	**[3.5 Internal Data RAM]** The internal data RAM is a 512-Kbyte RAM that can be accessed from the AHB and Header Endec.	3-4	**[3.5 Internal Data RAM]** The internal data RAM is a 512-Kbyte RAM. It is accessible by the AHB and Header Endec (communication bus).

No. 11 3.6 Buffer RAM

Access method to Buffer RAM corrected.

V8.00		V9.00	
Page	Description	Page	Description
3-6	**[3.6 Buffer RAM]** The buffer RAM is a 64-Kbyte RAM that can be accessed from the AHB and communication bus.	3-5	**[3.6 Buffer RAM]** The buffer RAM is a 64-Kbyte RAM. It is accessible by the communication bus.

No. 12 4. Bus Architecture

CC-Link added.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>4-1</td><td>[4. Bus Architecture]
[Table 4.1 AHB Internal Buses of the R-IN32M3]
<table><tr><td>Ethernet MAC Note 6</td><td>A</td><td>✓</td><td>—</td><td>✓</td><td>✓</td><td>—</td><td>Round robin (alternate) Note 3</td></tr><tr><td>APB internal peripheral modules Note 1</td><td>A</td><td>✓</td><td>—</td><td>✓</td><td>✓</td><td>—</td><td>Round robin (alternate) Note 3</td></tr></table></td><td>4-1</td><td>[4. Bus Architecture]
[Table 4.1 AHB Internal Buses of an R-IN32M3]
<table><tr><td>Ethernet MAC Note6</td><td>A</td><td>✓</td><td>—</td><td>✓</td><td>✓</td><td>—</td><td>Round robin (alternate) Note3</td></tr><tr><td>CC-Link<R></td><td>A</td><td>✓</td><td>—</td><td>✓</td><td>✓</td><td>—</td><td>Round robin (alternate) Note3</td></tr><tr><td>APB internal peripheral modules Note1</td><td>A</td><td>✓</td><td>—</td><td>✓</td><td>✓</td><td>—</td><td>Round robin (alternate) Note3</td></tr></table></td></tr>
</table>

No. 13 6.2 Semaphores

Number of semaphore identifiers corrected.

V8.00		V9.00	
Page	Description	Page	Description
6-1	**[6.2 Semaphores]** 125 semaphore identifiers can be handled.	6-1	**[6.2 Semaphores]** 128 semaphore identifiers can be handled.

No. 14 Deleted from Rev. 8.00: 6.6 Service Calls

Sub-Section [6.6 Service Calls] deleted.

V8.00		V9.00	
Page	Description	Page	Description
6-4 ~ 6-6	**[6.6 Service Calls]**	—	*(No entry)*

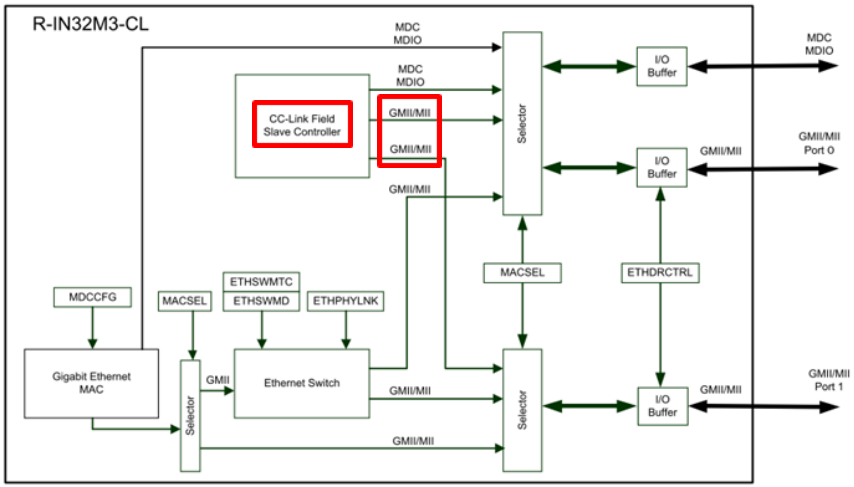
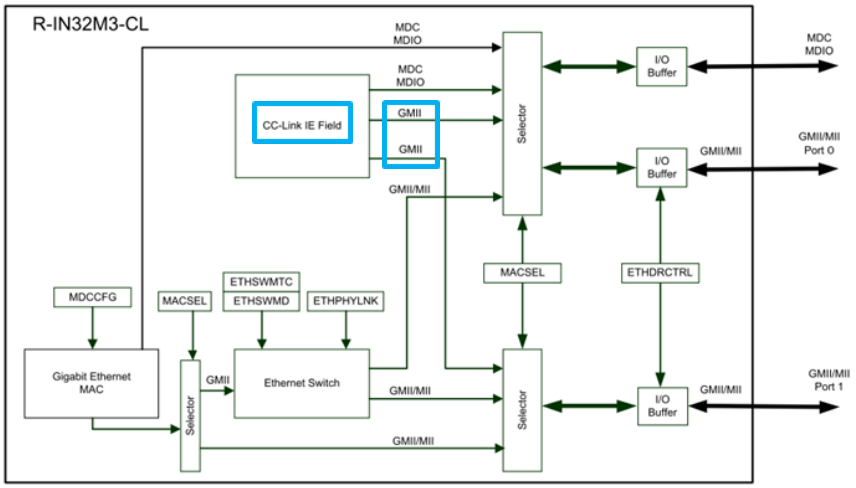
No. 15 7. Gigabit Ethernet MAC

Functional description about CC-Link IE Field of the R-IN32M3-CL corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-1	**[7. Gigabit Ethernet MAC]** Please refer to "R-IN32M3-EC User's Manual" and "R-IN32M3-CL User's Manual" respectively about the EtherCAT slave function of "R-IN32M3-EC" and the CC-Link IE Field slave function of "R-IN32M3-CL".	7-1	**[7. Gigabit Ethernet MAC]** Please refer to "R-IN32M3-EC User's Manual" and "R-IN32M3-CL User's Manual" respectively about the EtherCAT slave function of "R-IN32M3-EC" and the CC-Link IE Field function of "R-IN32M3-CL".

No. 16 7.1.1 Ethernet Interface Architecture

I/F between CC-Link IE Filed and Selector corrected. CC-Link Field Slave Controller changed to CC-Link IE Field.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-2</td><td>[7.1.1 Ethernet Interface Architecture]
[Figure 7.2 Ethernet Interface Peripheral Architecture (R-IN32M3-CL)]
 
</td><td>7-2</td><td>[7.1.1 Ethernet Interface Architecture]
[Figure 7.2 Ethernet Interface Peripheral Architecture (R-IN32M3-CL)]
 
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No. 17 7.3.1 (3) Gigabit Ethernet MAC control register

Numbering of MAC address registers corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-4
7-5</td><td>

[7.3.1 (3) Gigabit Ethernet MAC control register]

Pause packet register	GMAC_PAUSPKT	4009 009CH
MAC address register 0A	GMAC_ADR 0A	4009 0100H
MAC address register 0B	GMAC_ADR 0B	4009 0104H
MAC address register 1A	GMAC_ADR 1A	4009 0108H
MAC address register 1B	GMAC_ADR 1B	4009 010cH
MAC address register 2A	GMAC_ADR 2A	4009 0110H
MAC address register 2B	GMAC_ADR 2B	4009 0114H
MAC address register 3A	GMAC_ADR 3A	4009 0118H
MAC address register 3B	GMAC_ADR 3B	4009 011cH
MAC address register 4A	GMAC_ADR 4A	4009 0120H
MAC address register 4B	GMAC_ADR 4B	4009 0124H
MAC address register 5A	GMAC_ADR 5A	4009 0128H
MAC address register 5B	GMAC_ADR 5B	4009 012cH
MAC address register 6A	GMAC_ADR 6A	4009 0130H
MAC address register 6B	GMAC_ADR 6B	4009 0134H
MAC address register 7A	GMAC_ADR 7A	4009 0138H
MAC address register 7B	GMAC_ADR 7B	4009 013CH
MAC address register 8A	GMAC_ADR 8A	4009 0140H
MAC address register 8B	GMAC_ADR 8B	4009 0144H
MAC address register 9A	GMAC_ADR 9A	4009 0148H
MAC address register 9B	GMAC_ADR 9B	4009 014CH
MAC address register 10A	GMAC_ADR 10A	4009 0150H
MAC address register 10B	GMAC_ADR 10B	4009 0154H
MAC address register 11A	GMAC_ADR 11A	4009 0158H
MAC address register 11B	GMAC_ADR 11B	4009 015cH
MAC address register 12A	GMAC_ADR 12A	4009 0160H
MAC address register 12B	GMAC_ADR 12B	4009 0164H
MAC address register 13A	GMAC_ADR 13A	4009 0168H
MAC address register 13B	GMAC_ADR 13B	4009 016CH
MAC address register 14A	GMAC_ADR 14A	4009 0170H
MAC address register 14B	GMAC_ADR 14B	4009 0174H
MAC address register 15A	GMAC_ADR 15A	4009 0178H
MAC address register 15B	GMAC_ADR 15B	4009 017CH
RX FIFO status register	GMAC_RXFIFO	4009 0200H

</td><td>7-4
7-5</td><td>

[7.3.1 (3) Gigabit Ethernet MAC control registers]

Pause packet register	GMAC_PAUSPKT	4009 009CH
MAC address register 1A	GMAC_ADR 1A	4009 0100H
MAC address register 1B	GMAC_ADR 1B	4009 0104H
MAC address register 2A	GMAC_ADR 2A	4009 0108H
MAC address register 2B	GMAC_ADR 2B	4009 010cH
MAC address register 3A	GMAC_ADR 3A	4009 0110H
MAC address register 3B	GMAC_ADR 3B	4009 0114H
MAC address register 4A	GMAC_ADR 4A	4009 0118H
MAC address register 4B	GMAC_ADR 4B	4009 011cH
MAC address register 5A	GMAC_ADR 5A	4009 0120H
MAC address register 5B	GMAC_ADR 5B	4009 0124H
MAC address register 6A	GMAC_ADR 6A	4009 0128H
MAC address register 6B	GMAC_ADR 6B	4009 012CH
MAC address register 7A	GMAC_ADR 7A	4009 0130H
MAC address register 7B	GMAC_ADR 7B	4009 0134H
MAC address register 8A	GMAC_ADR 8A	4009 0138H
MAC address register 8B	GMAC_ADR 8B	4009 013CH
MAC address register 9A	GMAC_ADR 9A	4009 0140H
MAC address register 9B	GMAC_ADR 9B	4009 0144H
MAC address register 10A	GMAC_ADR 10A	4009 0148H
MAC address register 10B	GMAC_ADR 10B	4009 014CH
MAC address register 11A	GMAC_ADR 11A	4009 0150H
MAC address register 11B	GMAC_ADR 11B	4009 0154H
MAC address register 12A	GMAC_ADR 12A	4009 0158H
MAC address register 12B	GMAC_ADR 12B	4009 015cH
MAC address register 13A	GMAC_ADR 13A	4009 0160H
MAC address register 13B	GMAC_ADR 13B	4009 0164H
MAC address register 14A	GMAC_ADR 14A	4009 0168H
MAC address register 14B	GMAC_ADR 14B	4009 016CH
MAC address register 15A	GMAC_ADR 15A	4009 0170H
MAC address register 15B	GMAC_ADR 15B	4009 0174H
MAC address register 16A	GMAC_ADR 16A	4009 0178H
MAC address register 16B	GMAC_ADR 16B	4009 017CH
RX FIFO status register	GMAC_RXFIFO	4009 0200H

</td></tr>
</table>

No. 18 7.3.1 (3) Gigabit Ethernet MAC control register

Notes for the LPI mode control register and LPI client timing control register deleted.

V8.00		V9.00	
Page	Description	Page	Description
7-5	**[7.3.1 (3) Gigabit Ethernet MAC control register]** LPI mode control register Note LIP client timing control register Note Note: This is only available when the value of the MACSEL register is “0000 0002H” since the Ethernet switch does not support LPI mode.	7-5	**[7.3.1 (3) Gigabit Ethernet MAC control registers]** LPI mode control register LIP client timing control register *(No entry)*

No. 19 7.3.1 (4) Hardware function call register

Register name corrected. Registers added.

V8.00		V9.00	
Page	Description	Page	Description
7-5	**[7.3.1 (4) Hardware function call register]** Hardware function command register / SYSC / 4008 F000H Hardware function argument register 4 / R4 / 4008 F004H Hardware function argument register 5 / R5 / 4008 F008H Hardware function argument register 6 / R6 / 4008 F00CH Hardware function argument register 7 / R7 / 4008 F010H Hardware function return value register 0 / R0 / 4008 F020H Hardware function return value register 1 / R1 / 4008 F024H	7-5	**[7.3.1 (4) Hardware function call registers]** Hardware function system call register / SYSC / 4008 F000H Hardware function argument register 4 / R4 / 4008 F004H Hardware function argument register 5 / R5 / 4008 F008H Hardware function argument register 6 / R6 / 4008 F00CH Hardware function argument register 7 / R7 / 4008 F010H Hardware function operating mode control register / CMD / 4008 F014H Hardware function return value register 0 / R0 / 4008 F020H Hardware function return value register 1 / R1 / 4008 F024H Hardware function type register / CNTX_TYPE0 / 4008 0000H Hardware function state register / CNTX_STAT0 / 4008 0008H

No. 20 7.3.2.1 MAC Select Register (MACSEL)

Value corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-6	**[7.3.2.1 MAC Select Register (MACSEL)]** [Bit Position 2 to 0: MAC2 to MAC0] 010Note 3	7-6	**[7.3.2.1 MAC Select Register (MACSEL)]** [Bit Position 2 to 0: MAC2 to MAC0] 011Note3

No. 21 7.3.3.1 MDC Clock Select Register (MDCCFG)

Value corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-7	**[7.3.3.1 MDC Clock Select Register (MDCCFG)]** Caution 2. The setting of this register is only effective while the value of the MACSEL register is “0000 0000H” or “0000 0002H”.	7-7	**[7.3.3.1 MDC Clock Select Register (MDCCFG)]** Caution 2. The setting of this register is only effective while the value of the MACSEL register is “0000 0000H” or “0000 0003H”.

No. 22 7.3.4.1 MIIM Register (GMAC_MIIM)

Explicit bit names given.

V8.00		V9.00	
Page	Description	Page	Description
7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** 1. Start write operation: Set 1 to bit 26, PHY address to bits 25 to 21, PHY register address to bits 20 to 16, and write data to bits 15 to 0.	7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** 1. Start write operation: Set 1 to the RWDV bit, PHY address to the PHYADDR4 to 0 bits, PHY register address to the REGADDR4 to 0 bits, and write data to the DATA15 to 0 bits.

No. 23 7.3.4.1 MIIM Register (GMAC_MIIM)

Description numbering corrected. Explicit bit names given.

V8.00		V9.00	
Page	Description	Page	Description
7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** 4. Start read operation: Set 0 to bit 26, PHY address to bits 25 to 21, and PHY register address to bits 20 to 16.	7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** 1. Start read operation: Set 0 to the RWDV bit, PHY address to the PHYADDR4 to 0 bits, and PHY register address to the REGADDR4 to 0 bits.

No. 24 7.3.4.1 MIIM Register (GMAC_MIIM)

Caution corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** Caution: The setting of the MIIM register is only effective while the value of the MAC select register (MACSEL) is "0000 0000H" or "0000 0002H".	7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** Caution: The setting of this register is effective for the management interface selected by the MAC select register (MACSEL).

No. 25 7.3.4.1 MIIM Register (GMAC_MIIM)

Note modified.

V8.00		V9.00	
Page	Description	Page	Description
7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** Note 1. The RWDV bit after a reset indicates 1, but the DATA 15-0 bits do not indicate a valid value. It will indicate the correct state after the start processing of operation (writing to registers).	7-9	**[7.3.4.1 MIIM Register (GMAC_MIIM)]** Note. The RWDV bit becomes 1 after release from the reset state, but the settings of the DATA 15-0 bits are not effective at this time. When the RWDV bit is used to check the state of operation, start operation to read the correct state.

No. 26 7.3.4.2 TX ID Register (GMAC_TXID)

Description of the TX ID register added.

V8.00		V9.00	
Page	Description	Page	Description
7-10	**[7.3.4.2 TX ID Register (GMAC_TXID)]** *(No entry)*	7-10	**[7.3.4.2 TX ID Register (GMAC_TXID)]** This register indicates the ID of the transmission frame corresponding to the setting of the GMAC_TXRESULT register. To check the transmission frame result ID, be sure to read this register before reading the GMAC_TXRESULT register. If the GMAC_TXRESULT register is read first, the transmission frame result is updated and the updated transmission frame ID is read from this register.

No. 27 7.3.4.3 TX Result Register (GMAC_TXRESULT)

Description of the TX result register added.

V8.00		V9.00	
Page	Description	Page	Description
7-10	**[7.3.4.3 TX Result Register (GMAC_TXRESULT)]** *(No entry)*	7-10	**[7.3.4.3 TX Result Register (GMAC_TXRESULT)]** This register indicates the transmission frame result. The transmission frame result is updated when this register is read. The next time it is read, the updated transmission frame result can be read.

No. 28 7.3.4.3 TX Result Register (GMAC_TXRESULT)

Caution deleted.

V8.00		V9.00	
Page	Description	Page	Description
7-10	**[7.3.4.3 TX Result Register (GMAC_TXRESULT)]** Caution: Both the TX ID and TX result registers indicate the result of the transmission frame. These two registers are updated when the TX result register is read, and the transmission result of the next frame can be read. Therefore, the TX ID register must be read first before reading the TX result register (If the TX result register is read first, the frame ID read by the TX ID register indicates the TX ID for the next transmission result).	7-10	**[7.3.4.3 TX Result Register (GMAC_TXRESULT)]** *(No entry)*

No. 29 7.3.4.4 Mode Register (GMAC_MODE)

Description of the mode register added.

V8.00		V9.00	
Page	Description	Page	Description
7-11	**[7.3.4.4 Mode Register (GMAC_MODE)]** *(No entry)*	7-11	**[7.3.4.4 Mode Register (GMAC_MODE)]** This register is used to control the operating mode of the gigabit Ethernet MAC.

No. 30 7.3.4.4 Mode Register (GMAC_MODE)

Description of bit 31 ETHMODE expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-11	**[7.3.4.4 Mode Register (GMAC_MODE)]** [Bit Position 31: ETHMODE] Ethernet Mode 1: Operation is in Gigabit Ethernet mode.	7-11	**[7.3.4.4 Mode Register (GMAC_MODE)]** [Bit Position 31: ETHMODE] Ethernet Mode 1: Operation is in Gigabit Ethernet mode. Use this mode when the gigabit Ethernet MAC is connected the Ethernet switch.

No. 31 7.3.4.4 Mode Register (GMAC_MODE)

Description of bit 30 DUPMODE expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-11	**[7.3.4.4 Mode Register (GMAC_MODE)]** [Bit Position 30: DUPMODE] Duplex Mode 1: Operation is in Full duplex mode.	7-11	**[7.3.4.4 Mode Register (GMAC_MODE)]** [Bit Position 30: DUPMODE] Duplex Mode 1: Operation is in Full duplex mode. Use this mode when the gigabit Ethernet MAC is connected the Ethernet switch.

No. 32 7.3.4.5 RX Mode Register (GMAC_RXMODE)

Description of the RX mode register added.

V8.00		V9.00	
Page	Description	Page	Description
7-11	**[7.3.4.5 RX Mode Register (GMAC_RXMODE)]** *(No entry)*	7-11	**[7.3.4.5 RX Mode Register (GMAC_RXMODE)]** This register is used to control operation for reception of frames.

No. 33 7.3.4.5 RX Mode Register (GMAC_RXMODE)

Description of bit 30 MFILLTEREN corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-11	**[7.3.4.5 RX Mode Register (GMAC_RXMODE)]** [Bit Position 30: MFILLTEREN] Multicast Filtering Enable 1: Discard frames with multicast addresses other than those registered in the MAC address registers (GMAC_ADRnA, GMAC_ADRnB).	7-11	**[7.3.4.5 RX Mode Register (GMAC_RXMODE)]** [Bit Position 30: MFILLTEREN] Multicast Filtering Enable 1: Discard frames with multicast addresses other than those registered in the MAC address registers (GMAC_ADRnA, GMAC_ADRnB) (n = 1 to 16).

No. 34 7.3.4.6 TX Mode Register (GMAC_TXMODE)

Description of the TX mode register added.

V8.00		V9.00	
Page	Description	Page	Description
7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** *(No entry)*	7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** This register is used to control operation for transmission of frames.

No. 35 7.3.4.6 TX Mode Register (GMAC_TXMODE)

Bit 26 SFOP deleted.

V8.00		V9.00	
Page	Description	Page	Description
7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** - Bit field: Bit 26 = SFOP - R/W attribute: Bit 26 = R/W [Bit Position 26: SFOP] Store & Forward Option 1: A frame counter is used in the TX FIFO 0: A frame counter is not used in the TX FIFO	7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** - Bit field: Bit 26 = 0 - R/W attribute: Bit 26 = 0 *(No entry)*

No. 36 7.3.4.6 TX Mode Register (GMAC_TXMODE)

Note added to the description of bit 30 LPTXEN.

V8.00		V9.00	
Page	Description	Page	Description
7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** [Bit Position 30: LPTXEN] Long Packet TX Enable 1: Transmission of frames which exceed the length specified by the IEEE802.3 standard is enabled.	7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** [Bit Position 30: LPTXEN] Long Packet TX Enable 1: Transmission of frames which exceed the length specified by the IEEE802.3 standard is enabled.Note

No. 37 7.3.4.6 TX Mode Register (GMAC_TXMODE)

Note added.

V8.00		V9.00	
Page	Description	Page	Description
7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** *(No entry)*	7-13	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** Note: LPTXEN must be set to 1 since the frame size may exceed the maximum size of 1518 bytes while management tag insertion of the Ethernet switch is enabled (the SWTAGEN bit in the ETHSWMTC register is 1).

No. 38 7.3.4.6 TX Mode Register (GMAC_TXMODE)

Description of bits 7-6 TRBMODE1-0 modified.

V8.00		V9.00	
Page	Description	Page	Description
7-14	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** [Bit Position 7, 6: TRBMODE1-0] Transmission Result Buffer Mode Control how to write the transmission result to the TX result register. 00: Always writing 01: Writing only proceeds when an error occurs. 10: Writing does not proceed	7-14	**[7.3.4.6 TX Mode Register (GMAC_TXMODE)]** [Bit Position 7, 6: TRBMODE1-0] Transmission Result Buffer Mode Control how to write the transmission result to the GMAC_TXRESULT register. 00: Always writing 01: Writing only proceeds when an error occurs. 10: Writing does not proceed 11: Setting prohibited

No. 39 7.3.4.7 Reset Register (GMAC_RESET)

Description of the reset register added.

V8.00		V9.00	
Page	Description	Page	Description
7-14	**[7.3.4.7 Reset Register (GMAC_RESET)]** *(No entry)*	7-15	**[7.3.4.7 Reset Register (GMAC_RESET)]** This register is a trigger register for resetting the gigabit Ethernet MAC by software. The modules can be reset by setting the corresponding bit to 1. The value of the bit automatically returns to 0 afterward.

No. 40 7.3.4.7 Reset Register (GMAC_RESET)

Description of bit 31 ALLRST expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-14	**[7.3.4.7 Reset Register (GMAC_RESET)]** [Bit Position 31: ALLRST] All Ethernet MAC modules are reset. This bit returns to 0 automatically.	7-15	**[7.3.4.7 Reset Register (GMAC_RESET)]** [Bit Position 31: ALLRST] All Ethernet MAC modules are reset. 0: Reset completed 1: Reset the modules.

No. 41 7.3.4.7 Reset Register (GMAC_RESET)

Description of bit 15 TXRST expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-14	**[7.3.4.7 Reset Register (GMAC_RESET)]** [Bit Position 15: TXRST] The TX MAC, TX FIFO, and TX DMA modules are reset. This bit returns to 0 automatically.	7-15	**[7.3.4.7 Reset Register (GMAC_RESET)]** [Bit Position 15: TXRST] The TX MAC, TX FIFO, and TX DMA modules are reset. 0: Reset completed 1: Reset the modules.

No. 42 7.3.4.7 Reset Register (GMAC_RESET)

Description of bit 13 RXRST expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-14	**[7.3.4.7 Reset Register (GMAC_RESET)]** [Bit Position 13: RXRST] The RX MAC, RX FIFO, and RX DMA modules are reset. This bit returns to 0 automatically.	7-15	**[7.3.4.7 Reset Register (GMAC_RESET)]** [Bit Position 13: RXRST] The RX MAC, RX FIFO, and RX DMA modules are reset. 0: Reset completed 1: Reset the modules.

No. 43 7.3.4.8 Pause Packet Data Register (GMAC_PAUSEn)

Description of the pause register added.

V8.00		V9.00	
Page	Description	Page	Description
7-15	**[7.3.4.8 Pause Packet Data Register (GMAC_PAUSEn)]** *(No entry)*	7-16	**[7.3.4.8 Pause Packet Data Register (GMAC_PAUSEn)]** This register is used to specify a pause packet for transmission.

No. 44 7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)

Description of the RX flow control register added.

V8.00		V9.00	
Page	Description	Page	Description
7-16	**[7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)]** *(No entry)*	7-17	**[7.3.4.9 RX Flow Control Register (GMAC_FLWCTL)]** This register is used to control reception of a pause packet.

No. 45 7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)

Description of the pause packet register added.

V8.00		V9.00	
Page	Description	Page	Description
7-16	**[7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)]** *(No entry)*	7-18	**[7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)]** This register is used to control transmission of a pause packet. When 1 is written to the PPR bit, transmission of a pause packet starts. The bit is automatically set to 0 following the completion of the transmission.

No. 46 7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)

Description of bit 31 PPR modified.

V8.00		V9.00	
Page	Description	Page	Description
7-16	**[7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)]** [Bit Position 31: PPR] A pause packet is transmitted by writing ‘1’ to this bit. When the transmission of a pause packet ends, it returns to `0'.	7-18	**[7.3.4.10 Pause Packet Register (GMAC_PAUSPKT)]** [Bit Position 31: PPR] This bit controls transmission of a pause packet. 0: Nothing is to be done. 1: Start transmission of a pause packet.

No. 47 7.3.4.11 MAC Address Registers (GMAC_ADRnA, GMAC_ADRnB)

Description of the MAC address register corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-17	**[7.3.4.11 MAC Address Registers (GMAC_ADRnA, GMAC_ADRnB)]** These registers are used to configure the MAC addresses. A total of 16 MAC addresses can be registered. Bits 23 to 16 in the GMAC_ADRnB register can also be used to enable filtering of multiple addresses (n=0, 1, ..., 15).	7-19	**[7.3.4.11 MAC Address Registers (GMAC_ADRnA, GMAC_ADRnB)]** These registers are used to configure the MAC addresses. A total of 16 MAC addresses can be registered. Multiple addresses can be filtered by using the BITMSK7 to 0 bits of the GMAC_ADRnB register (n = 0, 2, ..., 16).

No. 48 7.3.4.11 MAC Address Registers (GMAC_ADRnA, GMAC_ADRnB)

Description of bits 23-16 BITMSK7-0 modified.

V8.00		V9.00	
Page	Description	Page	Description
7-17	**[7.3.4.11 MAC Address Registers (GMAC_ADRnA, GMAC_ADRnB)]** [Bit Position 23 to 16: BITMSK7-0] These bits mask given bits for matching in the comparison of DA[7:0]. Bits [23:16] of this register correspond to the DA [7:0] bits, respectively, and those for which the BITMSK setting is 0 are excluded from comparison for matching. For example, if mask register bits BITMSK2-0 are all 0, DA[2:0] are excluded from comparison for matching. In other words, if DA[47:3] match, the given frame is acquired.	7-19	**[7.3.4.11 MAC Address Registers (GMAC_ADRnA, GMAC_ADRnB)]** [Bit Position 23 to 16: BITMSK7-0] These bits mask given bits for matching in the comparison of the destination MAC address [7:0] bits. Bits [23:16] of this register correspond to the destination MAC address [7:0] bits, respectively, and those for which the BITMSK setting is 0 are excluded from comparison for matching. For example, if mask register bits BITMSK2-0 are all 0s, the destination MAC address [2:0] bits are excluded from comparison for matching. In other words, if the destination MAC address [47:3] bits match, the given frame is acquired.

No. 49 7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)

Description of the RX FIFO status register added.

V8.00		V9.00	
Page	Description	Page	Description
7-18	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** *(No entry)*	7-20	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** This register is a status register which indicates the state of the reception FIFO.

No. 50 7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)

Description of bit 31 RFULL modified.

V8.00		V9.00	
Page	Description	Page	Description
7-18	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [Bit Position 31: RFULL] RX FIFO Almost Full 1: Indicate that the data in the RX FIFO buffer is over the Receive Almost Full Threshold. (This threshold is configured by the RX mode register.)	7-20	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [Bit Position 31: RFULL] RX FIFO Almost Full 1: Indicate that the data in the RX FIFO buffer is over the Receive Almost Full Threshold. (This threshold is configured by the GMAC_RXMODE register.)

No. 51 7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)

Description of bit 30 REMP modified.

V8.00		V9.00	
Page	Description	Page	Description
7-18	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [Bit Position 30: REMP] RX FIFO Almost Empty 1: Indicate that the data in the RX FIFO buffer is below the Receive Almost Empty Threshold. (This threshold is configured by the RX mode register.)	7-20	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [Bit Position 30: REMP] RX FIFO Almost Empty 1: Indicate that the data in the RX FIFO buffer is below the Receive Almost Empty Threshold. (This threshold is configured by the GMAC_RXMODE register.)

No. 52 7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)

Description of bit 29 RRT modified.

V8.00		V9.00	
Page	Description	Page	Description
7-18	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [Bit Position 29: RRT] RX FIFO Read Trigger 1: Indicate that the data in the RX FIFO buffer is below the RX FIFO Read Threshold. (This threshold is configured by the RX mode register.)	7-20	**[7.3.4.12 RX FIFO Status Register (GMAC_RXFIFO)]** [Bit Position: 29 RRT] RX FIFO Read Trigger 1: Indicate that the data in the RX FIFO buffer is below the RX FIFO Read Threshold. (This threshold is configured by the GMAC_RXMODE register.)

No. 53 7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)

Description of the TX FIFO status register added.

V8.00		V9.00	
Page	Description	Page	Description
7-19	**[7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)]** *(No entry)*	7-21	**[7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)]** This register is a status register which indicates the state of the transmission FIFO.

No. 54 7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)

Bit 31 TFULL deleted.

V8.00		V9.00	
Page	Description	Page	Description
7-19	**[7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)]** - Bit field: Bit 31 = TFULL - R/W attribute: Bit 31 = R	7-21	**[7.3.4.13 TX FIFO Status Register (GMAC_TXFIFO)]** - Bit field: Bit 31 = 0 - R/W attribute: Bit 31 = 0

No. 55 7.3.4.14 TCPIPACC Register (GMAC_ACC)

Description of the TCPIPACC register added.

V8.00		V9.00	
Page	Description	Page	Description
7-20	**[7.3.4.14 TCPIPACC Register (GMAC_ACC)]** *(No entry)*	7-22	**[7.3.4.14 TCPIPACC Register (GMAC_ACC)]** This register is used to control operation of the TCPIP accelerator.

No. 56 7.3.4.14 TCPIPACC Register (GMAC_ACC)

Description of bit 2 RTCPIPACC expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-20	**[7.3.4.14 TCPIPACC Register (GMAC_ACC)]** [Bit Position 2: RTCPIPACC] 1: RX TCPIPACC Off Disable the checksum support of the RX TCPIP accelerator. Padding in the MAC header section is inserted.	7-22	**[7.3.4.14 TCPIPACC Register (GMAC_ACC)]** [Bit Position 2: RTCPIPACC] 1: RX TCPIPACC Off Disable the checksum support for the RX TCPIP accelerator. Padding in the MAC header section is inserted. 0: The checksum support for the RX TCPIP accelerator remains enabled.

No. 57 7.3.4.15 RX MAC Enable Register (GMAC_RXMAC_ENA)

Description of the RX MAC enable register added.

V8.00		V9.00	
Page	Description	Page	Description
7-20	**[7.3.4.15 RX MAC Enable Register (GMAC_RXMAC_ENA)]** *(No entry)*	7-22	**[7.3.4.15 RX MAC Enable Register (GMAC_RXMAC_ENA)]** This register is used to control operation of the reception MAC.

No. 58 7.3.4.16 LPI mode control register (GMAC_LPI_MODE)

Description of the LPI mode control register added.

V8.00		V9.00	
Page	Description	Page	Description
7-21	**[7.3.4.16 LPI mode control register (GMAC_LPI_MODE)]** *(No entry)*	7-23	**[7.3.4.16 LPI mode control register (GMAC_LPI_MODE)]** This register is used control LPI (Low Power Idle) mode. If the Gigabit Ethernet MAC is connected via the Ethernet switch, do not use this register to set LPI mode.

No. 59 7.3.4.17 LPI Client Timing Control Register (GMAC_LPI_TIMING)

Description of the LPI client timing control register added.

V8.00		V9.00	
Page	Description	Page	Description
7-21	**[7.3.4.17 LPI Client Timing Control Register (GMAC_LPI_TIMING)]** *(No entry)*	7-23	**[7.3.4.17 LPI Client Timing Control Register (GMAC_LPI_TIMING)]** This register is used to control the signal timing in LPI mode. Do not use this register if the Gigabit Ethernet MAC is connected via the Ethernet switch.

No. 60 7.3.4.17 LPI Client Timing Control Register (GMAC_LPI_TIMING)

Value in Caution for the LPI client timing control register corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-21	**[7.3.4.17 LPI Client Timing Control Register (GMAC_LPI_TIMING)]** Caution: The settings of the GMAC_LPI_MODE and GMAC_PLI_TIMING registers are effective while the MACSEL register value is 0000 0002H.	7-23	**[7.3.4.17 LPI Client Timing Control Register (GMAC_LPI_TIMING)]** Caution: The settings of the GMAC_LPI_MODE and GMAC_LPI_TIMING registers are effective while the MACSEL register value is 0000 0003H.

No. 61 7.3.4.18 Receive Buffer Information Register (BUFID)

R/W attribute corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-22	**[7.3.4.18 Receive Buffer Information Register (BUFID)]** - R/W attribute: Bit 31 = R/W - R/W attribute: Bit[28:0] = R/W	7-24	**[7.3.4.18 Receive Buffer Information Register (BUFID)]** - R/W attribute: Bit 31 = R - R/W attribute: Bit[28:0] = R

No. 62 7.3.4.18 Receive Buffer Information Register (BUFID)

Note added.

V8.00		V9.00	
Page	Description	Page	Description
7-22	**[7.3.4.18 Receive Buffer Information Register (BUFID)]** *(No entry)*	7-24	**[7.3.4.18 Receive Buffer Information Register (BUFID)]** Note: Since this register indicates the information of the next received data every time it is read, the value of this register changes every time it is read.

No. 63 7.3.5 Hardware Function Call Register

Description of hardware function call register modified.

V8.00		V9.00	
Page	Description	Page	Description
7-23	**[7.3.5 Hardware Function Call Register]** The hardware function call register is used to acquire buffers and start transmission or reception (hardware function). The hardware function is executed by writing the given command to the command register (SYSC) after configuring the argument registers (R4-R7).	7-25	**[7.3.5 Hardware Function Call Register]** The hardware function call registers are used to acquire buffers and start transmission or reception (hardware function). The hardware function is executed by writing the given command to the system call register (SYSC) after configuring the argument registers (R4 to R7). For how to configure the hardware function call registers, see section 7.4.1, Hardware Functions.

No. 64 7.3.5.1 Hardware Function Command Register (SYSC)

Functions of the hardware function system call register added and corrected. Note deleted.

V8.00		V9.00	
Page	Description	Page	Description
7-23	**[7.3.5.1 Hardware Function Command Register (SYSC)]** [Bit Position 15 to 0: SYSC15-0] 0x5000 Acquire buffers 0x5100 Start transmission 0x5101 Start reception Others Setting prohibited Note: The hardware function related registers are also used for controlling the hardware OS accelerator.	7-25	**[7.3.5.1 Hardware Function Command Register (SYSC)]** [Bit Position 15 to 0: SYSC15-0] 0x5000 Acquires a long buffer. 0x5006 Acquires a short buffer. 0x5001 Releases the whole area of the buffer. 0x5002 Releases the part of the buffer. 0x5101 Enables DMA for the reception MAC. 0x5102 Disables DMA for the reception MAC. 0x510B Controls interrupts for the reception MACDMAC. 0x510D Obtains error sources for the reception MACDMAC. 0x5100 Starts transfer by the transmission MACDMAC. 0x510C Obtains error sources in the transmission MACDMAC. 0x5211 Starts DMA transfer between the buffer RAM and data RAM. 0x5212 Starts replacing data in the buffer RAM or data RAM. 0x5104 Starts DMA transfer between the buffer RAMs. 0x5114 Starts DMA transfer between the buffer RAMs (descriptor method). Others Setting prohibited *(No entry)*

No. 65 7.3.5.2 Hardware Function Argument Registers (R4 to 7)

Description of the hardware function argument register expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-24	**[7.3.5.2 Hardware Function Argument Registers (R4-7)]** These registers are for writing arguments transferred to a hardware function. Which register is used differs with the hardware function.	7-26	**[7.3.5.2 Hardware Function Argument Registers (R4 to R7)]** These registers are for writing arguments transferred to a hardware function. Which register is used differs with the hardware function. For details, see section 7.4, Functions.

No. 66 7.3.5.3 Hardware Function Operating Mode Control Register (CMD)

Hardware function operating mode control register added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-27	**[7.3.5.3 Hardware Function Operating Mode Control Register (CMD)]**

No. 67 7.3.5.4 Hardware Function Return Value Registers (R0, R1)

Description of the hardware function return value register expanded.

V8.00		V9.00	
Page	Description	Page	Description
7-25	**[7.3.5.3 Hardware Function Return Value Registers (R0, R1)]** These registers indicate the returned value from a hardware function. The meaning of the returned value depends on the hardware function.	7-28	**[7.3.5.4 Hardware Function Return Value Registers (R0, R1)]** These registers hold the value returned from a hardware function. The value returned depends on the hardware function. For details, see section 7.4, Functions.

No. 68 7.3.5.5 Hardware Function Type Register (CNTX_TYPE0)

Hardware function type register added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-28	[7.3.5.5 Hardware Function Type Register (CNTX_TYPE0)]

No. 69 7.3.5.6 Hardware Function State Register (CNTX_STAT0)

Hardware function state register added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-29	[7.3.5.6 Hardware Function State Register (CNTX_STAT0)]

No. 70 7.4.1 Hardware Functions

Hardware functions added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-30	[7.4.1 Hardware Functions]

No. 71 7.4.1.1 Initial Settings

Initial settings added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-31	[7.4.1.1 Initial Settings]

No. 72 7.4.1.2 Flow of Processing for Issuing the Hardware Function Call

Flow chart expanded.

<table>
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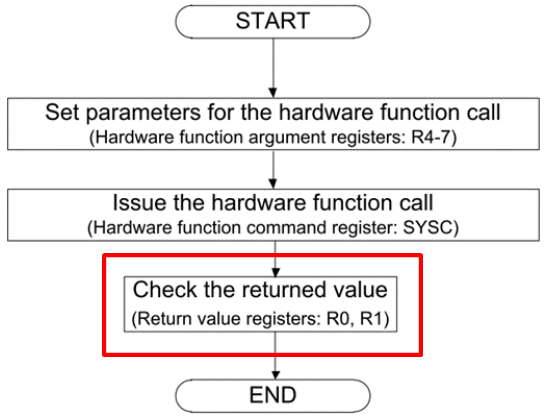
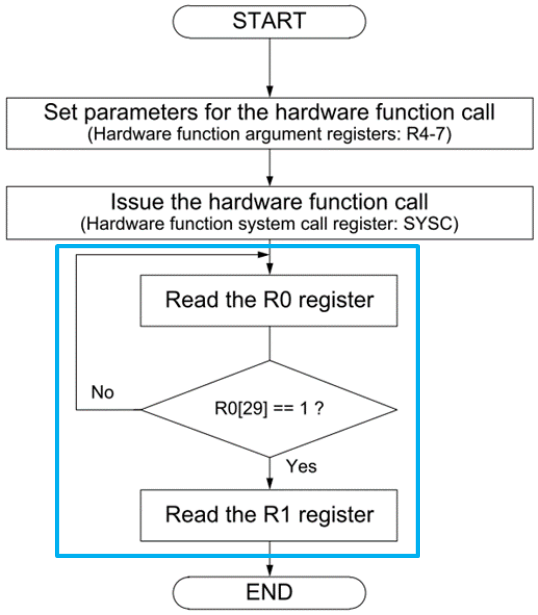
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>7-26</td><td>[7.3.5.4 Hardware Function Call Issue Processing Flow]
[Figure 7.3 Hardware Function Call Issue Processing Flow]
 
</td><td>7-31</td><td>[7.4.1.2 Flow of Processing for Issuing the Hardware Function Call]
[Figure 7.4 Flow of Processing for Issuing the Hardware Function]
 
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No. 73 7.4.1.3 Buffer Allocator

Buffer allocator added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-32	**[7.4.1.3 Buffer Allocator]**

No. 74 7.4.1.4 MAC DMA Controller

MAC DMA controller added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-39	**[7.4.1.4 MAC DMA Controller]**

No. 75 7.4.1.5 Buffer RAM DMA Controller

Buffer RAM DMA controller added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-50	**[7.4.1.5 Buffer RAM DMA Controller]**

No. 76 7.4.2 Interrupts

Interrupts added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	7-55	**[7.4.2 Interrupts]**

No. 77 Deleted from Rev. 8.00: 7.4.1.1 Initial Settings

Initial settings sub-section deleted.

V8.00		V9.00	
Page	Description	Page	Description
7-27	**[7.4.1.1 Initial Settings]** At first, write 0x8000 0000 to the RESET register (→ 7.3.4.7) to reset the MAC. Make initial settings for the following registers. • MAC address register (→ 7.3.4.11) • TX MODE register (→ 7.3.4.6) • RX MODE register (→ 7.3.4.5)	7-57	*(No entry)*

No. 78 7.4.3.1 Acquiring a Transmit Buffer

Description of R0 corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-28	**[7.4.1.2 Acquiring a Transmit Buffer]** [Register: R0 (bit 15 to bit 0)] 0x0001,0x0000: Securing of the memory completed Others : Error (failure in securing the memory block)	7-58	**[7.4.3.1 Acquiring a Transmit Buffer]** [Register: R0] 0xb and R0[29] = 1: Success 2'b10: Invalid system call 2'b11: The buffer is insufficient.

No. 79 7.4.3.2 Creating TX Data

Description modified and changed to Caution style.

V8.00		V9.00	
Page	Description	Page	Description
7-29	**[7.4.1.3 Creating TX data]** • If the above format is not followed, the operation is undefined. • Padding (2 bytes) can be by any value. • The padding (2 bytes) is not included in the specified size of Ethernet frames (TX_WORD[12:0], TX_EOB[1:0]).	7-59	**[7.4.3.2 Creating TX Data]** Cautions 1. Make sure that the TX data conforms to this format. 2. Padding (2 bytes) can be by any value. Padding (2 bytes) is not included in the specified size of Ethernet frames (TX_WORD[12:0], TX_EOB[1:0]).

No. 80 Deleted from Rev. 8.00: 7.4.2.1 Initial Settings

Initial settings sub-section deleted.

V8.00		V9.00	
Page	Description	Page	Description
7-33	**[7.4.2.1 Initial Settings]** Reset the MAC and make initial settings for the registers as in section 7.4.1.1.	7-63	*(No entry)*

No. 81 7.4.4.5 Rx Data Format

Number of bytes for Padding corrected.

V8.00		V9.00	
Page	Description	Page	Description
7-34	**[7.4.2.6 Rx Data Format]** Padding (0 to 3 bytes)	7-64	**[7.4.4.5 Rx Data Format]** Padding (0 to 7 bytes)

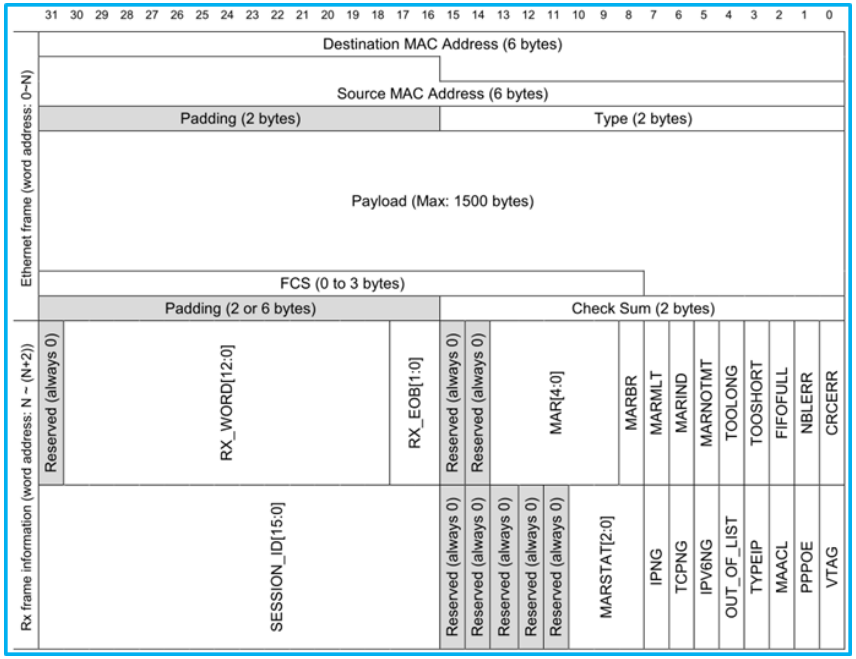
No. 82 7.4.4.5 Rx Data Format

Definition (for Frames without the TPC/IP and UDP/IP Packets) added to the figure title.

V8.00		V9.00	
Page	Description	Page	Description
7-34	**[7.4.2.6 Rx Data Format]** [Figure 7.6 RX Data Format]	7-64	**[7.4.4.5 Rx Data Format]** [Figure 7.15 Format of Receive Data for Frames without the TPC/IP and UDP/IP Packets]

No. 83 7.4.4.5 Rx Data Format

Figure 7.16 added.

V8.00		V9.00	
Page	Description	Page	Description
7-34	**[7.4.2.6 Rx Data Format]** *(No entry)*	7-65	**[7.4.4.5 Rx Data Format]** [Figure 7.16 Format of Receive Data for Frames with the TPC/IP and UDP/IP Packets] 

No. 84 8.3.1 (2) Switch Configuration Registers

Name of input learning blocking register corrected.

V8.00		V9.00	
Page	Description	Page	Description
8-3	**[8.3.1 (2) Switch configuration registers]** Input learning blocking register INPUT_LERAN_BLOCK	8-3	**[8.3.1 (2) Switch Configuration Registers]** Input learning blocking register INPUT_LEARN_BLOCK

No. 85 8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

Description of Ethernet PHY LINK mode register expanded.

V8.00		V9.00	
Page	Description	Page	Description
8-6	**[8.3.2.1 Ethernet PHY LINK mode register (ETHPHYLNK)]** This register is used to specify the active level of Ethernet PHY LINK signal. This register can be read and written in 32- or 16-bit units.	8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** This register is used to specify the active level of the Ethernet PHY LINK signals. Set this register according to the active level of the PHYLINK signal from an external PHY to be connected. This register can be read or written in 32- or 16-bit units.

No. 86 8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

Caution 2 added.

V8.00		V9.00	
Page	Description	Page	Description
8-6	**[8.3.2.1 Ethernet PHY LINK mode register (ETHPHYLNK)]** Caution: This register is only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register.	8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** Cautions 1. This register is only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register. 2. Since the Ethernet PHY of the R-IN32M3-EC operates according to the setting of the initial value, leave the value at the initial value.

No. 87 8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

Description of bit 3 CATLINK1 modified.

V8.00		V9.00	
Page	Description	Page	Description
8-6	**[8.3.2.1 Ethernet PHY LINK mode register (ETHPHYLNK)]** [Bit Position 3: CATLINK1] Specify the active level of the PHYLINK1 signal using EtherCAT interface. 1: Active-Low PHYLINK signal (initial). 0: Active-High PHYLINK signal.	8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** [Bit Position 3: CATLINK1] This bit sets the active level of the PHYLINK signal for port 1 of the EtherCAT interface. 1: The PHYLINK signal is active high. 0: The PHYLINK signal is active low (initial value).

No. 88 8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

Description of bit 2 CATLINK0 modified.

V8.00		V9.00	
Page	Description	Page	Description
8-6	**[8.3.2.1 Ethernet PHY LINK mode register (ETHPHYLNK)]** [Bit Position 2: CATLINK0] Specify the active level of the PHYLINK0 signal using EtherCAT interface. 1: Active-Low PHYLINK signal (initial). 0: Active-High PHYLINK signal.	8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** [Bit Position 2: CATLINK0] This bit sets the active level of the PHYLINK signal for port 0 of the EtherCAT interface. 1: The PHYLINK signal is active high. 0: The PHYLINK signal is active low (initial value).

No. 89 8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

Description of bit 1 SWLINK1 modified.

V8.00		V9.00	
Page	Description	Page	Description
8-6	**[8.3.2.1 Ethernet PHY LINK mode register (ETHPHYLNK)]** [Bit Position 1: SWLINK1] Specify the active level of the LINK1 signal using Ethernet Switch interface. 1: Active-Low PHYLINK signal. 0: Active-High PHYLINK signal (initial).	8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** [Bit Position 1: SWLINK1] This bit sets the active level of the PHYLINK signal for port 1 of the Ethernet switch interface. 1: The PHYLINK signal is active low (initial value) 0: The PHYLINK signal is active high.

No. 90 8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

Description of bit 0 SWLINK0 modified.

V8.00		V9.00	
Page	Description	Page	Description
8-6	**[8.3.2.1 Ethernet PHY LINK mode register (ETHPHYLNK)]** [Bit Position 0: SWLINK0] Specify the active level of the LINK1 signal using Ethernet Switch interface. 1: Active-Low PHYLINK signal. 0: Active-High PHYLINK signal (initial).	8-6	**[8.3.2.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)]** [Bit Position 0: SWLINK0] This bit sets the active level of the PHYLINK signal for port 0 of the Ethernet switch interface. 1: The PHYLINK signal is active low (initial value) 0: The PHYLINK signal is active high.

No. 91 8.3.3.5 Input Learning Blocking Register (INPUT_LEARN_BLOCK)

Name of the input learning blocking register corrected.

V8.00		V9.00	
Page	Description	Page	Description
8-14	**[8.3.3.5 Input learning blocking register (INPUT_LERAN_BLOCK)]** - Register name: INPUT_LERAN_BLOCK	8-14	**[8.3.3.5 Input Learning Blocking Register (INPUT_LEARN_BLOCK)]** - Register name: INPUT_LEARN_BLOCK

No. 92 8.5.2 Switch Initialization

Values in table corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>8-89</td><td>[8.5.2 Switch hardware initialization]
[Table 8.19 Initial settings of address table]
<table>
<tr><th>Address</th><th>Register</th><th>Initial Setting</th><th>Description</th></tr>
<tr><td>4007 4000H to 4007 47FC (4-byte units)</td><td>ADR_TABLE</td><td>0000 0000H</td><td>Initialize all entries to 0 in the address table.</td></tr>
<tr><td>4007 4000H + Hash value of Unicast MAC address × 8H</td><td>ADR_TABLE</td><td>0403 0201H</td><td>Set as static entry unicast address.
Setting example is 01-02-03-04-05-06.
Only mask port2 with priority 0.
Setting is not required when set dynamically.</td></tr>
<tr><td>Address above+4H</td><td>ADR_TABLE</td><td>0083 0605</td><td></td></tr>
</table></td><td>8-96</td><td>[8.5.2 Switch Initialization]
[Table 8.19 Examples of Initial Settings of the Address Table]
<table>
<tr><th>Address</th><th>Register</th><th>Example Setting</th><th>Description</th></tr>
<tr><td>4007 4000H to 4007 47FCH (4-byte units)</td><td>ADR_TABLE</td><td>0000 0000H</td><td>Initialize all entries to 0 in the address table.</td></tr>
<tr><td>4007 4000H + Hash value of Unicast MAC address × 8H</td><td>ADR_TABLE</td><td>0403 0201H</td><td>Set a unicast address as a static entry.
The example settings are when the MAC address is 01-02-03-04-05-06. The priority level is 0 and only port 2 is masked.
These settings are not required when set dynamically.</td></tr>
<tr><td>Address above + 4H</td><td>ADR_TABLE</td><td>0083 0605H</td><td></td></tr>
</table></td></tr>
</table>

No. 93 8.5.2 Switch Initialization

Values in table corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>8-90</td><td>[8.5.2 Switch hardware initialization]
[Table 8.20 Initialization settings of switch engine]
<table>
<tr><td>4007 0020H</td><td>MGMT_CONFIG</td><td>000 0042H</td><td>Enable accepting BPDU frames (bit6=1) and force them to be forwarded to the management port (value 2 in bits 3:0) If management frames should be discarded bit 7 should be set instead of bit 6.</td></tr>
<tr><td>4007 0100H
4007 0104H
4007 0108H</td><td>VLAN_PRIORITY0
VLAN_PRIORITY1
VLAN_PRIORITY2</td><td>006D B688H</td><td>Initialize VLAN priority mapping into the 4 queues available in the hardware for each port. It maps priorities 0..3 into queues 0..3 and priorities 4..7 all into queue 3.</td></tr>
<tr><td>4007 0180H
4007 0184H
4007 0188H</td><td>PRIORITY_CFG0
PRIORITY_CFG1
PRIORITY_CFG2</td><td>000 0001H</td><td>Enable VLAN priority classification for each port and set default port priority to 0.</td></tr>
</table></td><td>8-97</td><td>[8.5.2 Switch Initialization]
[Table 8.20 Examples of Initial Settings of the Switch Engine]
<table>
<tr><td>4007 0020H</td><td>MGMT_CONFIG</td><td>0000 0042H</td><td>Enables reception of BPDU frames (bit 6 = 1) to transfer them to the management port (port 2) If management frames should be discarded, bit 7 should be set to 1.</td></tr>
<tr><td>4007 0100H
4007 0104H
4007 0108H</td><td>VLAN_PRIORITY0
VLAN_PRIORITY1
VLAN_PRIORITY2</td><td>006D B688H</td><td>Map VLAN priority into the 4 queues available for each port. In this setting, priorities 0 to 3 are mapped into queues 0 to 3 and priorities 4 to 7 all into queue 3.</td></tr>
<tr><td>4007 0180H
4007 0184H
4007 0188H</td><td>PRIORITY_CFG0
PRIORITY_CFG1
PRIORITY_CFG2</td><td>0000 0001H</td><td>Enable mapping of the output queue by VLAN priority classification for each port and set default port priority to 0.</td></tr>
</table></td></tr>
</table>

No. 94 9. Asynchronous SRAM Memory Controller (ROM/SRAM)

Caution expanded.

V8.00		V9.00	
Page	Description	Page	Description
9-1	**[9. Asynchronous SRAM Memory Controller (ROM/SRAM)]** Caution: Do not change the setting of the MEMCSEL pin during operation. Fix the setting before release from the reset state.	9-1	**[9. Asynchronous SRAM Memory Controller (ROM/SRAM)]** Caution: Do not change the setting of the operating mode setting pins such as the MEMIFSEL and MEMCSEL pins during operation. Fix the setting before release from the reset state.

No. 95 9.2 (1) (a) SRAM and external I/O connection

Maximum allowable number of idle wait cycles corrected.

V8.00		V9.00	
Page	Description	Page	Description
9-2	**[9.2 (1) (a) SRAM and external I/O connection]** • An idle wait of up to 15 BUSCLK cycles can be inserted by setting the relevant register.	9-2	**[9.2 (1) (a) SRAM and external I/O connection]** • An idle wait of up to 16 BUSCLK cycles can be inserted by setting the relevant register.

No. 96 9.2 (1) (b) Page ROM connection

Maximum allowable number of idle wait cycles corrected.

V8.00		V9.00	
Page	Description	Page	Description
9-2	**[9.2 (1) (b) Page ROM connection]** • An idle wait of up to 15 BUSCLK cycles can be inserted by setting the relevant register.	9-2	**[9.2 (1) (b) Page ROM connection]** • An idle wait of up to 16 BUSCLK cycles can be inserted by setting the relevant register.

No. 97 9.3.3 Static Memory Control Registers 0 to 3 (SMC0 to SMC3)

WEZ corrected to WRZn.

V8.00		V9.00	
Page	Description	Page	Description
9-6	**[9.3.3 Static Memory Control Registers 0 to 3 (SMC0 to SMC3)]** [Bit Position 11 to 8: WWn3-WWn0] Set a write recovery wait for each CSZn. A write recovery wait is the cycle from de-assertion of WRSTBZ and WRZn (WEZ: L → H) to de-assertion of CSZn (CSZn: L → H).	9-6	**[9.3.3 Static Memory Control Registers 0 to 3 (SMC0 to SMC3)]** [Bit Position 11 to 8: WWn3-WWn0] Set a write recovery wait for each CSZn. A write recovery wait is the cycle from de-assertion of WRSTBZ and WRZn (WRZn: L → H) to de-assertion of CSZn (CSZn: L → H).

No. 98 9.3.3 Static Memory Control Registers 0 to 3 (SMC0 to SMC3)

REZ and WEZ corrected to RDZ and WRZn.

V8.00		V9.00	
Page	Description	Page	Description
9-6	**[9.3.3 Static Memory Control Registers 0 to 3 (SMC0 to SMC3)]** [Bit Position 7 to 4: DWn3-DWn0] Set a data wait for each CSZn. In the case of no wait, REZ and WEZ having a width of 1 cycle of BUSCLK are extended by the number of wait cycles set for the data wait.	9-6	**[9.3.3 Static Memory Control Registers 0 to 3 (SMC0 to SMC3)]** [Bit Position 7 to 4: DWn3-DWn0] Set a data wait for each CSZn. In the case of no wait, RDZ and WRZn having a width of 1 cycle of BUSCLK are extended by the number of wait cycles set for the data wait.

No. 99 9.3.5 Write Enable Switching Register (WREN)

[3:0] changed to 0-3.

V8.00		V9.00	
Page	Description	Page	Description
9-11	**[9.3.5 Write Enable Switching Register (WREN)]** This register selects WRZ [3:0] or BENZ [3:0] for the BENZ [3:0] pin function. The WREN register can be read and written in 32-bit units. The register is set to 0000 0001H by a reset and the BENZ [3:0] pins operate as WRZ [3:0].	9-11	**[9.3.5 Write Enable Switching Register (WREN)]** This register selects WRZ3-WRZ0 or BENZ3-BENZ0 for the BENZ3-BENZ0 pin function. The WREN register can be read or written in 32-bit units. The register is set to 0000 0001H by a reset and the BENZ3-BENZ0 pins operate as WRZ3-WRZ0.

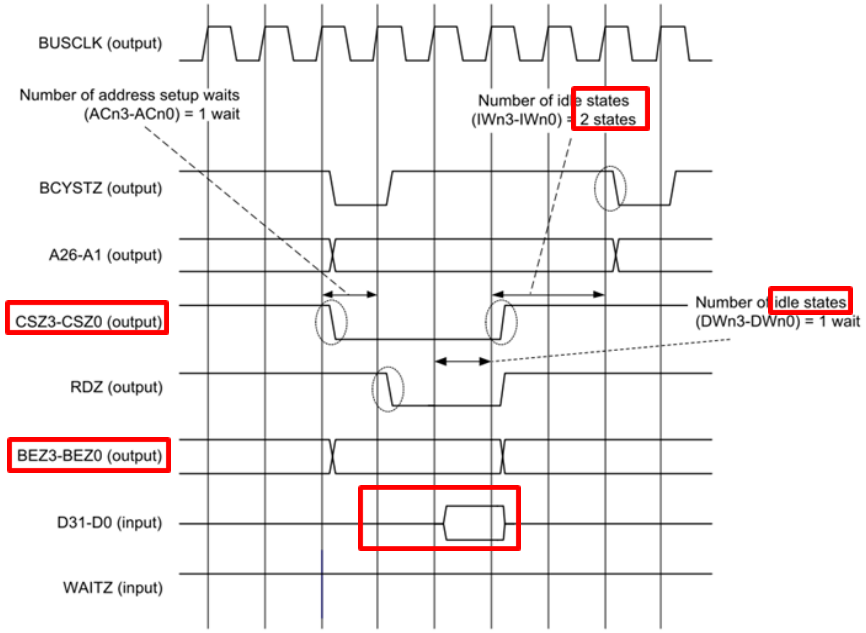
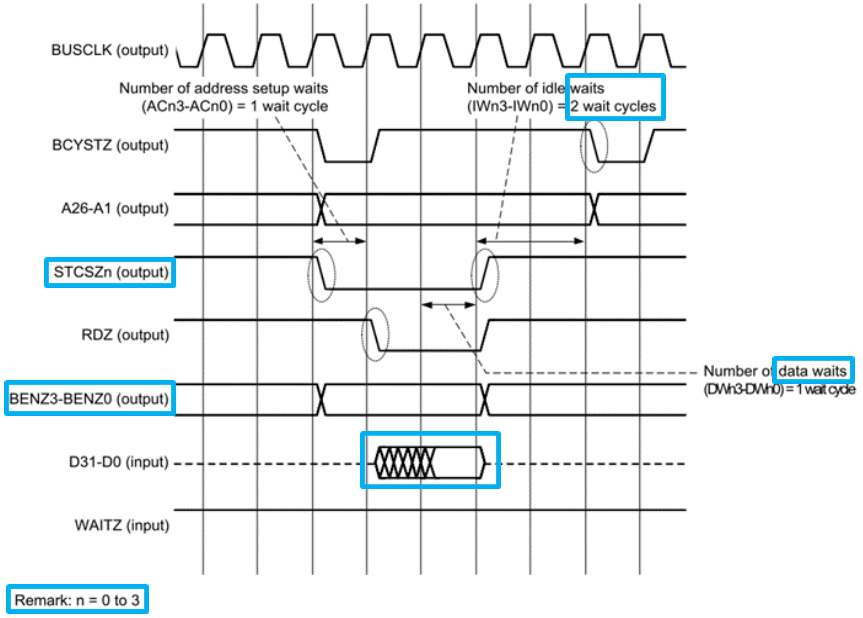
No. 100 9.7 Memory Access Timing Examples

State(s) corrected to wait cycle(s) in the descriptions above figures 9.8, 9.9, 9.10, and 9.15.

V8.00		V9.00	
Page	Description	Page	Description
9-17 ~ 9-24	**[9.7 Memory Access Timing Examples]** *(Description above Figure 9.8 SRAM Read Cycles)* BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: IWn3-IWn0 = 0000B (1 state) *(Description above Figure 9.9 SRAM Read Cycles (with Wait Settings))* BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: IWn3-IWn0 = 0001B (2 states) *(Description above 9.10 SRAM Read Cycles (External Wait Insertion))* BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: IWn3-IWn0 = 0000B (1 state) *(Description above Figure 9.15 Page ROM Read Cycles (Four Burst Transfer))* BSC: SBS3-SBS0 = 1111B (32 bits), SMC0 :IW03-IW00 = 0001B (2 states)	9-17 ~ 9-24	**[9.7 Memory Access Timing Examples]** *(Description above Figure 9.8 SRAM Read Cycles)* BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: IWn3-IWn0 = 0000B (1 wait cycle) *(Description above Figure 9.9 SRAM Read Cycles (with Wait Settings))* BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: IWn3-IWn0 = 0001B (2 wait cycles) *(Description above 9.10 SRAM Read Cycles (External Wait Insertion))* BSC: SBS3-SBS0 = 1111B (32 bits), SMCn: IWn3-IWn0 = 0000B (1 wait cycle) *(Description above Figure 9.15 Page ROM Read Cycles (Four Burst Transfer))* BSC: SBS3-SBS0 = 1111B (32 bits), SMC0 :IW03-IW00 = 0001B (2 wait cycles)

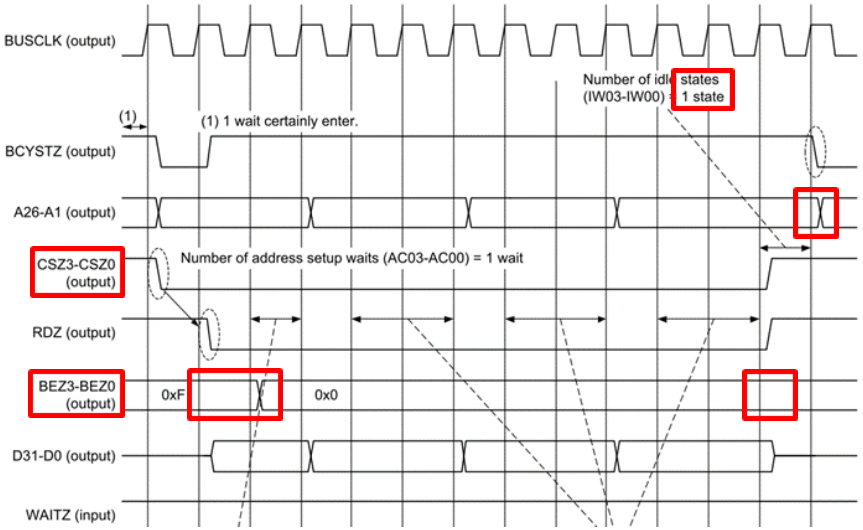
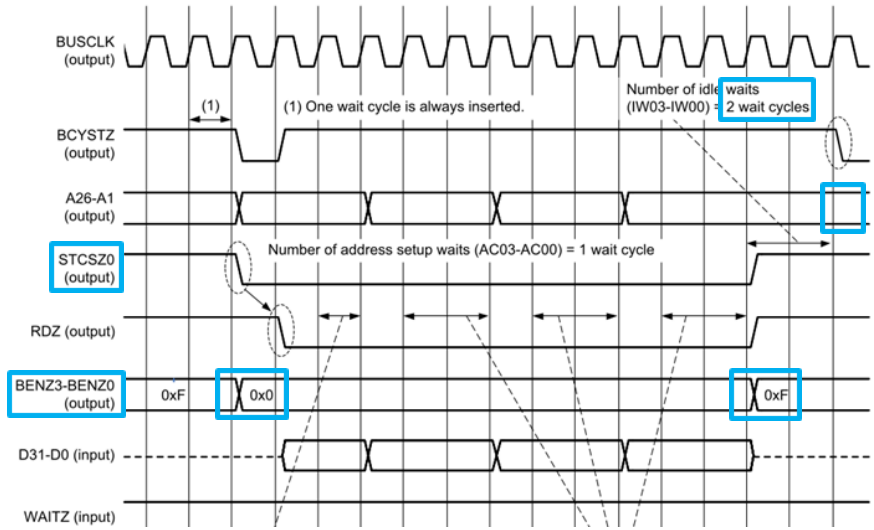
No. 101 9.7 Memory Access Timing Examples

States in figure 9.9 corrected to waits or wait cycles. Signal names corrected. Timing chart modified. Remark added.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>9-18</td><td>[9.7 Memory Access Timing Examples]
[Figure 9.9 SRAM Read Cycles (with Wait Settings)]
 
</td><td>9-18</td><td>[9.7 Memory Access Timing Examples]
[Figure 9.9 SRAM Read Cycles (with Wait Settings)]
 
</td></tr>
</table>

No. 102 9.7 Memory Access Timing Examples

States corrected to waits. "1 state" corrected to "2 wait cycles". Signal names corrected. Timing charts modified.

V8.00		V9.00	
Page	Description	Page	Description
9-24	**[9.7 Memory Access Timing Examples]** [Figure 9.15 Page ROM Read Cycles (Four Burst Transfer)] 	9-24	**[9.7 Memory Access Timing Examples]** [Figure 9.15 Page ROM Read Cycles (Four Burst Transfer)] 

No. 103 10. Synchronous Burst Access Memory Controller

Caution expanded.

V8.00		V9.00	
Page	Description	Page	Description
10-1	**[10. Synchronous Burst Access Memory Controller]** Caution: Do not change the setting of the MEMCSEL and ADMUXMODE pins during operation. Fix the setting before the reset period ends.	10-1	**[10. Synchronous Burst Access Memory Controller]** Caution: Do not change the setting of the operating mode setting pins such as the MEMCSEL and ADMUXMODE pins during operation. Fix the setting before the reset period ends.

No. 104 10.1 Features

Names of wait signals corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-1	**[10.1 Features]** • Static memory control - Up to four wait signals (WAITZ0 to WAITZ3) can be used.	10-1	**[10.1 Features]** • Static memory control - Up to four wait signals (WAITZ, WAITZ1 to WAITZ3) can be used.

No. 105 10.1 Features

CLK_OUT for masking corrected to BUSCLK.

V8.00		V9.00	
Page	Description	Page	Description
10-2	**[10.1 Features]** • CLK_OUT masking - Output the CLK_OUT signal.	10-2	**[10.1 Features]** • BUSCLK signal masking - Output the BUSCLK signal only while the CSZx signal is active.

No. 106 10.1 Features

WE_n and CS corrected to WRZx and CSZx.

V8.00		V9.00	
Page	Description	Page	Description
10-2	**[10.1 Features]** • Write enable control - Output the WE_n signal. - Keep the WE_n signal active while the CS signal is active.	10-2	**[10.1 Features]** • Write enable control *(No entry)* - Keep the WRZx signal active while the CSZx signal is active.

No. 107 10.1 Features

CLK_OUT for read timing control corrected to BUSCLK.

V8.00		V9.00	
Page	Description	Page	Description
10-2	**[10.1 Features]** • Data read timing and WAIT signal - Read data and latch the WAIT signal at the rising edge of CLK_OUT. - Read data and latch the WAIT signal at the falling edge of CLK_OUT.	10-2	**[10.1 Features]** • Control of data read timing: Read data and WAIT signal - Read data and the WAITZx signal are taken in at the rising edge of BUSCLK. - Read data and the WAITZx signal are taken in at the falling edge of BUSCLK.

No. 108 10.2 Control registers

Symbols in table corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-3</td><td>[10.2 Control registers]
[Table 10.1 Synchronous burst access memory controller control registers]
<table>
<tr><td>SMC operating mode setting register</td><td>SMCMD</td><td>4001 0124H</td></tr>
<tr><td>SMC direct command register</td><td>DIRECTCMD</td><td>400A 8010H</td></tr>
<tr><td>SMC cycle setting register</td><td>SETCYCLES</td><td>400A 8014H</td></tr>
<tr><td>SMC mode setting register</td><td>SETOPMODE</td><td>400A 8018H</td></tr>
<tr><td>SMC refresh setting register</td><td>REFRESH_0</td><td>400A 8020H</td></tr>
</table></td><td>10-3</td><td>[10.2 Control registers]
[Table 10.1 Synchronous Burst Access Memory Controller Control Registers]
<table>
<tr><td>SMC operating mode setting register</td><td>SMC352MD</td><td>4001 0124H</td></tr>
<tr><td>SMC direct command register</td><td>DIRECT_CMD</td><td>400A 8010H</td></tr>
<tr><td>SMC cycle setting register</td><td>SET_CYCLES</td><td>400A 8014H</td></tr>
<tr><td>SMC mode setting register</td><td>SET_OPMODE</td><td>400A 8018H</td></tr>
<tr><td>SMC refresh setting register</td><td>REF_PERIOD0</td><td>400A 8020H</td></tr>
</table></td></tr>
</table>

Note: Change of register names is error. The names will be returned to the old names in the next revision.

No. 109 10.2.1 WAITZ Selection Register (WAITZSEL)

WAITZ0 to WAITZ3 pins corrected to WAITZ1 to WAITZ3 pins.

V8.00		V9.00	
Page	Description	Page	Description
10-4	**[10.2.1 WAITZ selection register (WAITZSEL)]** This register is used to enable or disable the signals input from the WAITZ0 to WAITZ3 pins to the CSZ0 to CSZ3 areas.	10-4	**[10.2.1 WAITZ Selection Register (WAITZSEL)]** This register is used to enable or disable the signals input from the WAITZ pin and the WAITZ1 to WAITZ3 pins to the CSZ0 to CSZ3 areas.

No. 110 10.2.1 WAITZ Selection Register (WAITZSEL)

Names of WSELmn bits and WAITZm signals modified.

V8.00		V9.00	
Page	Description	Page	Description
10-4	**[10.2.1 WAITZ selection register (WAITZSEL)]** [Bit Position 15 to 0: WSELmn] Specify whether to enable the WAITZ input signal for each CSZ area. 0000: Use the WAITZm pin as the WAIT pin Remark: m = 0 to 3, n = 0 to 3	10-4 10-5	**[10.2.1 WAITZ Selection Register (WAITZSEL)]** [Bit Position 15 to 12: WSEL3n] Specify whether to enable the WAITZ3 input signal for each CSZ area. 0000: Use the WAITZ3 pin as the WAIT pin [Bit Position 11 to 8: WSEL2n] Specify whether to enable the WAITZ2 input signal for each CSZ area. 0000: Use the WAITZ2 pin as the WAIT pin [Bit Position 7 to 4: WSEL1n] Specify whether to enable the WAITZ1 input signal for each CSZ area. 0000: Use the WAITZ1 pin as the WAIT pin [Bit Position 3 to 0: WSEL0n] Remark: n = 0 to 3

No. 111 10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)

Names of bits 3-0 corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-6	**[10.2.2 Synchronous burst access memory controller area select registers (SMADSEL0 to SMADSEL3)]** [Bit Position 3 to 0: SMCSnMASK3 to SMCSnMASK0]	10-7	**[10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)]** [Bit Position 3 to 0: SMCSnSIZE3 to SMCSnSIZE0]

No. 112 10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)

Remark modified.

V8.00		V9.00	
Page	Description	Page	Description
10-6	**[10.2.2 Synchronous burst access memory controller area select registers (SMADSEL0 to SMADSEL3)]** Remark: Example of address area calculation Base address ([31:24]) = access address [31:24] and mask value [7:0]	10-7	**[10.2.2 Synchronous Burst Access Memory Controller Area Select Registers (SMADSEL0 to SMADSEL3)]** Remark: Example of address area calculation Base address ([31:24]) = access address [31:24] and size value [7:0]

No. 113 10.2.4 Synchronous Burst Access Memory Controller Operation Setting Register (SMC352MD)

Register name corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-8	**[10.2.4 Synchronous burst access memory controller operation setting register (SMCMD)]** - Register name: SMCMD	10-9	**[10.2.4 Synchronous Burst Access Memory Controller Operation Setting Register (SMC352MD)]** - Register name: SMC352MD

Note: Change of register name is error. The name will be returned to the old name (SMCMD) in the next revision.

No. 114 10.2.4 Synchronous Burst Access Memory Controller Operation Setting Register (SMC352MD)

Description of bit 1 SMCWETH corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-8	**[10.2.4 Synchronous burst access memory controller operation setting register (SMCMD)]** [Bit Position 1: SMCWETH] Select the SRAM WE_n output mode. 0: Output as is. 1: After WE_n is asserted, SRAM WE_n stays active while the CS signal is active.	10-9	**[10.2.4 Synchronous Burst Access Memory Controller Operation Setting Register (SMC352MD)]** [Bit Position 1: SMCWETH] Select the SRAM WRZn output mode. 0: SRAM WRZn stays active during the period specified by the T_WP bit of the SET_CYCLE register. 1: After WRZn is asserted, SRAM WRZn stays active while the CS signal is active.

No. 115 10.2.4 Synchronous Burst Access Memory Controller Operation Setting Register (SMC352MD)

Pin name in Note 1 corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-8	**[10.2.4 Synchronous burst access memory controller operation setting register (SMCMD)]** Note 1. This register becomes effective only when an ADMAXMODE terminal is high-level.	10-9	**[10.2.4 Synchronous Burst Access Memory Controller Operation Setting Register (SMC352MD)]** Note 1. This register becomes effective only when an ADMUXMODE terminal is high-level.

No. 116 10.2.6 Cycle Setting Register (SET_CYCLE)

Description of bits 13-11 T_WP corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-10	**[10.2.6 Cycle setting register (SET_CYCLE)]** [Bit Position 13 to 11: T_WP] If the SMCWETH bit of the SMCMD register is 1, the WRSTBZ signal remains active while the CS signal is active, regardless of the value set to the T_WP signal.	10-11	**[10.2.6 Cycle Setting Register (SET_CYCLE)]** [Bit Position 13 to 11: T_WP] If the SMCWETH bit of the SMC352MD register is 1, the WRSTBZ signal remains active while the CS signal is active, regardless of the value set to the T_WP signal.

No. 117 10.2.8 Synchronous Burst Access Memory Controller Refresh Setting Register (REF_PERIOD0)

Address value corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-14	**[10.2.8 Synchronous burst access memory controller refresh setting register (REF_PERIOD0)]** - Address: 400A 8018H	10-15	**[10.2.8 Synchronous Burst Access Memory Controller Refresh Setting Register (REF_PERIOD0)]** - Address: 400A 8020H

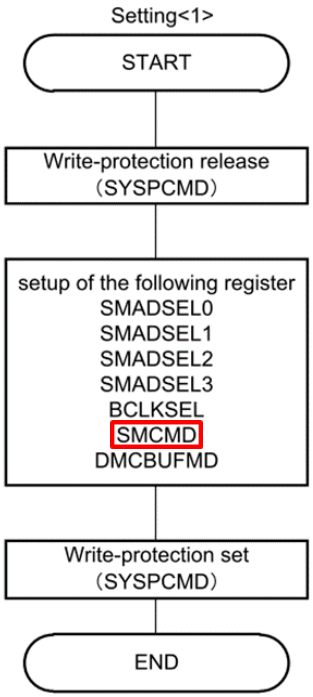
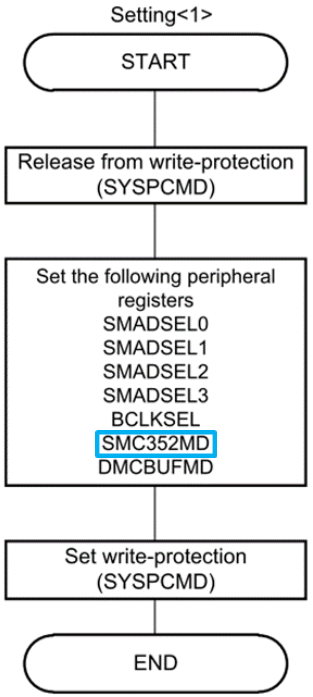
No. 118 10.2.10 Synchronous Burst Access Memory Controller CSn Mode Registers (OPMODE0_n)

Description of bits 15-0 corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-16	**[10.2.10 Synchronous burst access memory controller CSn mode registers (OPMODE0_0 to OPMODE03)]** [Bit Position 15 to 0: –] The value set to SETOPMODE can be read.	10-16	**[10.2.10 Synchronous Burst Access Memory Controller CSn Mode Registers (OPMODE0_n)]** [Bit Position 15 to 0: –] The value set to SET_OPMODE can be read.

No. 119 10.2.11 Register Setup Procedure

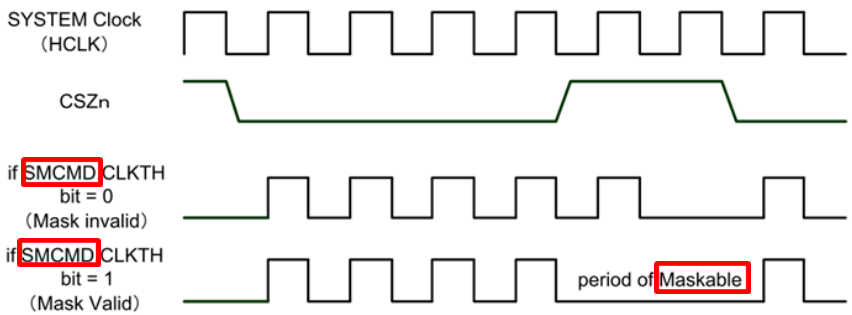
Register name in figure corrected.

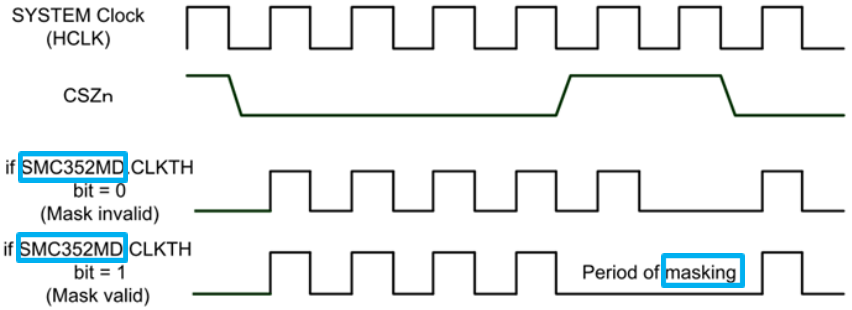
<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-17</td><td>[10.2.11 Register setup procedure]
[Figure 10.1 Register setup procedure]
 
</td><td>10-17</td><td>[10.2.11 Register Setup Procedure]
[Figure 10.1 Register Setup Procedure]
 
</td></tr>
</table>

No. 120 10.3.1 Bus Clock Selection

Register name in figure corrected. Typo fixed.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-18</td><td>[10.3.1 Bus clock selection]
The bus clock (BUSCLK) can be output for the period in which the CSZn signal is active, which is specified by the SMCMD register.

[Figure 10.2 Bus clock mask operation]
 
</td><td>10-18</td><td>[10.3.1 Bus Clock Selection]
The bus clock (BUSCLK) can be output for the period in which the CSZn signal is active, which is specified by the SMC352MD register.

[Figure 10.2 Bus Clock Mask Operation]
 
</td></tr>
</table>

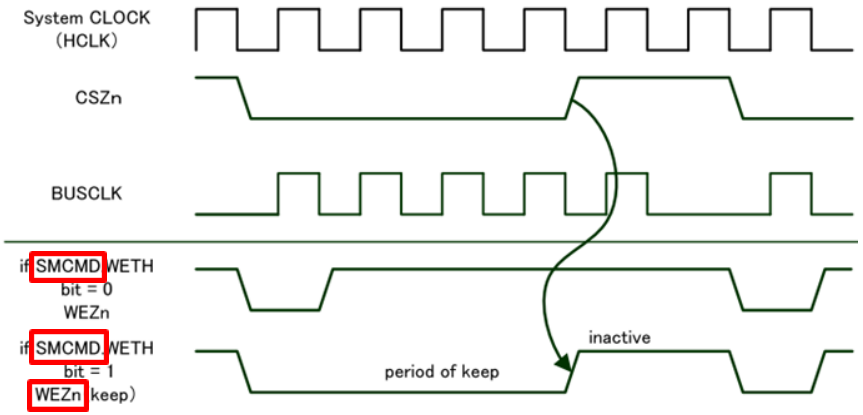
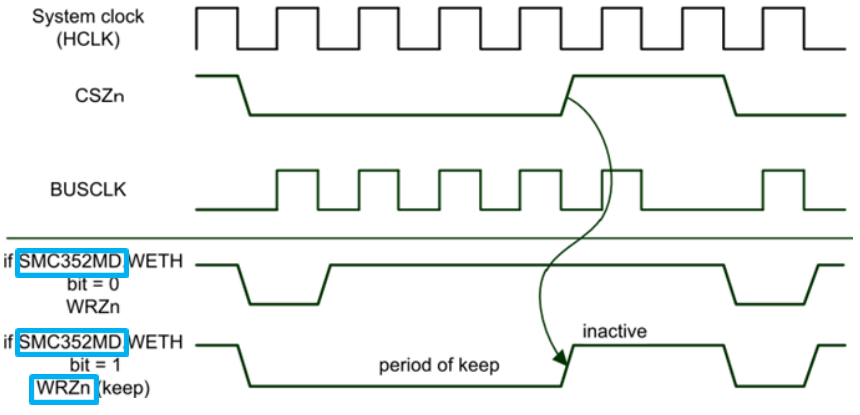
No. 121 10.3.3 Address/Data Multiplexing Feature

Matrix of address/data multiplexing feature deleted.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-19</td><td>[10.3.3 Address/data multiplexing feature]
<table>
<tr><th rowspan="2">External SRAM pins</th><th colspan="2">In separate bus mode (ADMUXMODE = 0)</th><th colspan="2">In multiplexed bus mode (ADMUXMODE = 1)</th><th rowspan="2">Remark</th></tr>
<tr><th>16-bit bus mode</th><th>32-bit bus mode</th><th>16-bit bus mode</th><th>32-bit bus mode</th></tr>
<tr><td>A27 to A1</td><td>Address27 to Address1</td><td>Address28 to Address2</td><td>Address27 to Address1</td><td>Address28 to Address2</td><td>The address signal is output regardless of the mode.</td></tr>
<tr><td>D31 to D16</td><td>–</td><td>Data31 to Data16</td><td>Address31 to Address16</td><td>{2'b0,Address29 to Address2}</td><td rowspan="2">For the address output timing in multiplexed bus mode, see “Figure 10.7”</td></tr>
<tr><td>D15 to D0</td><td>Data15 to Data0</td><td>Data15 to Data0</td><td>Address16 to Address1
Data15 to Data0</td><td>Data31 to Data0</td></tr>
</table></td><td>10-19</td><td>[10.3.3 Address/Data Multiplexing Feature]
(No entry)</td></tr>
</table>

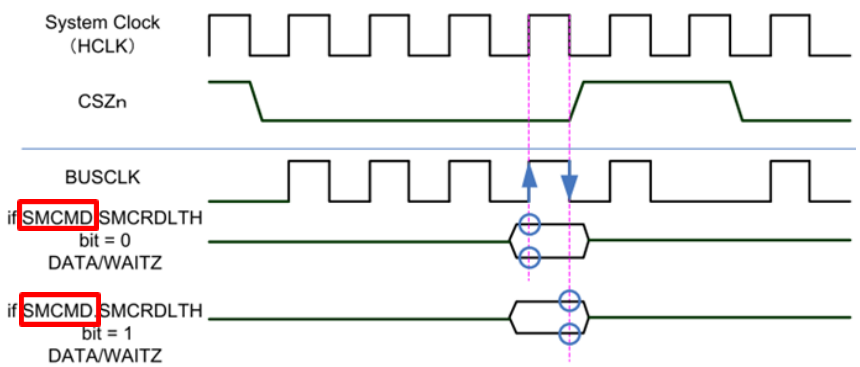
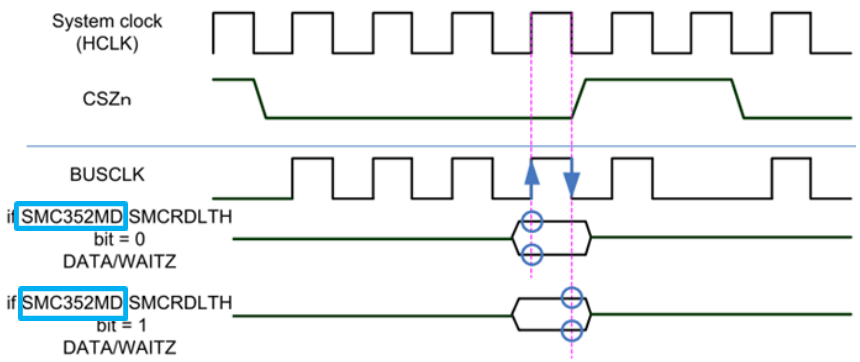
No. 122 10.3.4 Write Enable Signal (WRZn) Cycle Extension

Write enable pin name in the description and figure corrected. Register names in figure corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>10-19</td><td>[10.3.4 Write enable signal (WEZn) cycle extension]
The write enable pin (WEZn) of the synchronous burst access memory controller is output only in the first cycle after the CSZn signal is asserted when performing synchronous access. Some external peripheral devices cannot receive the write enable signal (WEZn) within one cycle. To solve this problem, the active period of the write enable signal (WEZn) can be extended while the chip select signal (CSZn) is active. To enable this feature, set the SMCWETH bit of the SMCMD register to 1.
 
</td><td>10-19</td><td>[10.3.4 Write Enable Signal (WRZn) Cycle Extension]
The write enable pin (WRZn) of the synchronous burst access memory controller is output only in the first cycle after the CSZn signal is asserted when performing synchronous access. Some external peripheral devices cannot receive the write enable signal (WRZn) within one cycle. To solve this problem, the active period of the write enable signal (WRZn) can be extended while the chip select signal (CSZn) is active. To enable this feature, set the SMCWETH bit of the SMC352MD register to 1.
 
</td></tr>
</table>

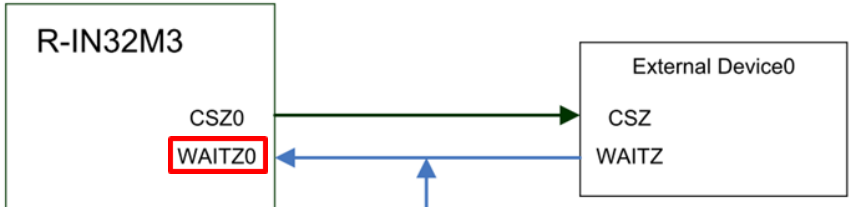
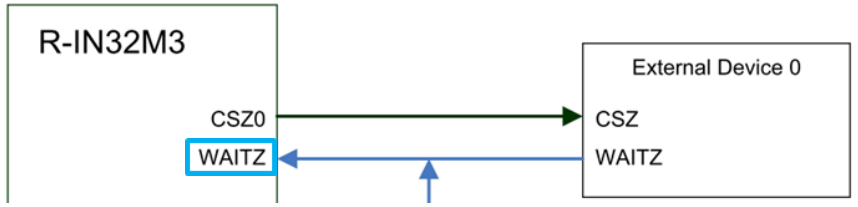
No. 123 10.3.5 Controlling the Data Read Timing

Register names in figure corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-20	**[10.3.5 Controlling the data read timing]** 	10-20	**[10.3.5 Controlling the Data Read Timing]** 

No. 124 10.3.6 (1) Connection example 1

Description of connection example 1 and figure corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-21	**[10.3.6 (1) Connection example 1]** Four external devices are connected. The WAIT signals are connected by using WAITZ0 via wired OR logic. 	10-21	**[10.3.6 (1) Connection example 1]** Four external devices are connected. The WAIT signals are connected by using WAITZ via wired OR logic. 

No. 125 10.3.6 (2) Connection example 2

Figure of connection example 2 corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-22	**[10.3.6 (2) Connection example 2]** 	10-22	**[10.3.6 (2) Connection example 2]** 

No. 126 10.3.6 (3) Connection example 3

Figure of connection example 3 corrected.

V8.00		V9.00	
Page	Description	Page	Description
10-23	**[10.3.6 (3) Connection example 3]** 	10-23	**[10.3.6 (3) Connection example 3]** 

No. 127 10.4.2 Synchronous Access Timing

Caution added.

V8.00		V9.00	
Page	Description	Page	Description
10-41	**[10.4.2 Synchronous access timing]** *(No entry)*	10-42	**[10.4.2 Synchronous Access Timing]** Caution: Do not change the setting of the operating mode setting pins such as the MEMIFSEL and MEMCSEL pins during operation. Fix the setting before release from the reset state.

No. 128 11. External MCU Interface

Caution added.

V8.00		V9.00	
Page	Description	Page	Description
11-1	**[11. External MCU Interface]** *(No entry)*	11-1	**[11. External MCU Interface]** Caution: Do not change the setting of the operating mode setting pins such as the MEMIFSEL and MEMCSEL pins during operation. Fix the setting before release from the reset state.

No. 129 11.2.5 (2) HOSTIF bus control register (HIFBCC)

Remark modified and changed to Caution style.

V8.00		V9.00	
Page	Description	Page	Description
11-18	**[11.2.5 (2) HOSTIF Bus control register (HIFBCC)]** Remark: In the above-mentioned area, there is an area of the outside for prediction in part.	11-18	**[11.2.5 (2) HOSTIF bus control register (HIFBCC)]** Caution: Some areas cannot be read in advance depending on the target macro even if advance reading is enabled.

No. 130 11.3.2 Selection of Operational Mode

Caution added.

V8.00		V9.00	
Page	Description	Page	Description
11-27	**[11.3.2 Selection of Operational Mode]** *(No entry)*	11-27	**[11.3.2 Selection of Operational Mode]** Caution: With a synchronous SRAM type transfer mode, the asynchronous interface cannot be selected.

No. 131 11.3.4 (2) HOSTIF synchronous SRAM control register 0 (HIFEXT0)

Caution added.

V8.00		V9.00	
Page	Description	Page	Description
11-29	**[11.3.4 (2) HOSTIF synchronous SRAM control register0 (HIFEXT0)]** *(No entry)*	11-29	**[11.3.4 (2) HOSTIF synchronous SRAM control register 0 (HIFEXT0)]** Caution: Do not write a value other than 0 to the bits fixed to 0. Writing any other value to these bits may lead to a malfunction.

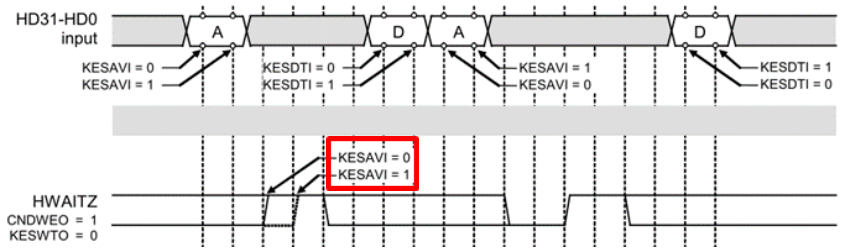
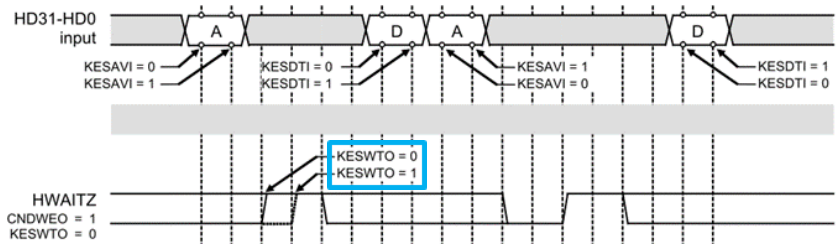
No. 132 11.3.4 (3) HOSTIF synchronous SRAM control register 1 (HIFEXT1)

Caution added.

V8.00		V9.00	
Page	Description	Page	Description
11-30	**[11.3.4 (3) HOSTIF synchronous SRAM control register1 (HIFEXT1)]** *(No entry)*	11-30	**[11.3.4 (3) HOSTIF synchronous SRAM control register 1 (HIFEXT1)]** Caution: Do not write a value other than 0 to the bits fixed to 0. Writing any other value to these bits may lead to a malfunction.

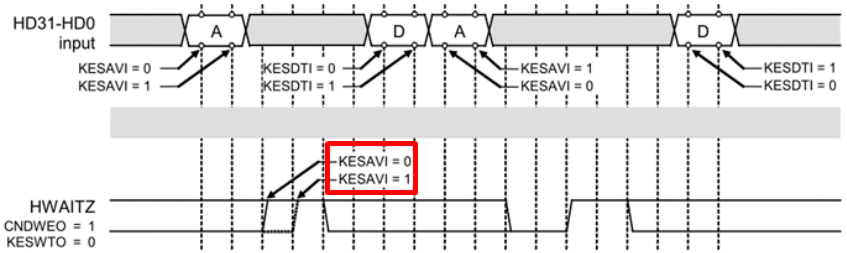
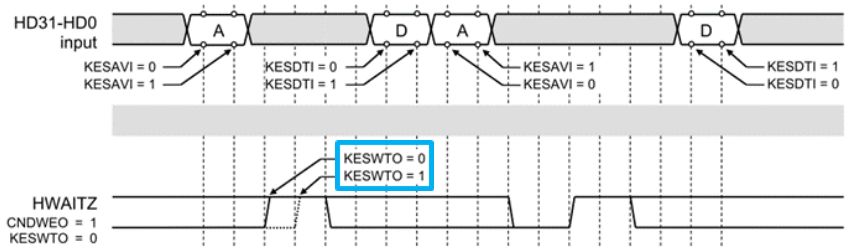
No. 133 11.3.5 (1) Write access by the external MCU (synchronous SRAM single transfer, multiplexing of addresses and data, write status)

Title of sub-section modified. KESAVI in the figure corrected to KESWTO.

V8.00		V9.00	
Page	Description	Page	Description
11-31	**[11.3.5 (1) Write access from external microprocessor (synchronous SRAM Single transmission, Address/Data multiplex, write status)]** 	11-31	**[11.3.5 (1) Write access by the external MCU (synchronous SRAM single transfer, multiplexing of addresses and data, write status)]** 

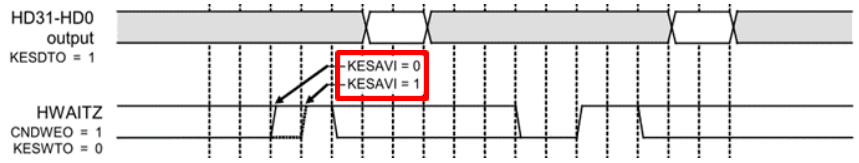
No. 134 11.3.5 (2) Write access by the external MCU (synchronous SRAM single transfer, multiplexing of addresses and data, write strobe)

Title of sub-section modified. KESAVI in the figure corrected to KESWTO.

V8.00		V9.00	
Page	Description	Page	Description
11-32	**[11.3.5 (2) Write access from external microprocessor (synchronous SRAM Single transmission, Address/Data multiplex, write strobe)]** 	11-32	**[11.3.5 (2) Write access by the external MCU (synchronous SRAM single transfer, multiplexing of addresses and data, write strobe)]** 

No. 135 11.3.5 (3) Read access by the external MCU (synchronous SRAM single transfer, multiplexing of addresses and data)

Title of sub-section modified. KESAVI in the figure corrected to KESWTO.

V8.00		V9.00	
Page	Description	Page	Description
11-33	**[11.3.5 (3) Read access from external microprocessor (synchronous SRAM single transmission, Address/Data multiplex)]** 	11-33	**[11.3.5 (3) Read access by the external MCU (synchronous SRAM single transfer, multiplexing of addresses and data)]** 

No. 136 Section 12 All

SMCLK corrected to SMSCK in the entirety of Section 12.

V8.00		V9.00	
Page	Description	Page	Description
12-1 ~ 12-24	**[Section 12 All]** SMCLK	12-1 ~ 12-25	**[Section 12 All]** SMSCK

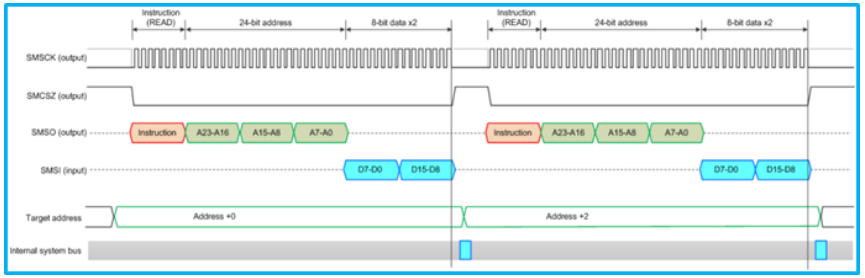
No. 137 12.2.1 Transfer Mode Control Register (SFMSMD)

Register name corrected.

V8.00		V9.00	
Page	Description	Page	Description
12-3	**[12.2.1 Transfer Mode Control Register (SFMSMD)]** SFMSMD0	12-3	**[12.2.1 Transfer Mode Control Register (SFMSMD)]** SFMSMD

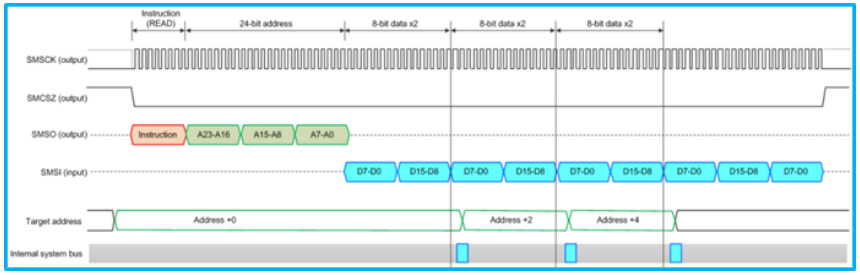
No. 138 12.4.4 (1) ROM Reading by Individual Conversion

[Figure 12.14 Continuous Data Reading by Individual Conversion] added.

V8.00		V9.00	
Page	Description	Page	Description
12-21	**[12.4.4 (1) ROM reading by individual conversion]** *(No entry)*	12-21	**[12.4.4 (1) ROM Reading by Individual Conversion]** [Figure 12.14 Continuous Data Reading by Individual Conversion] 

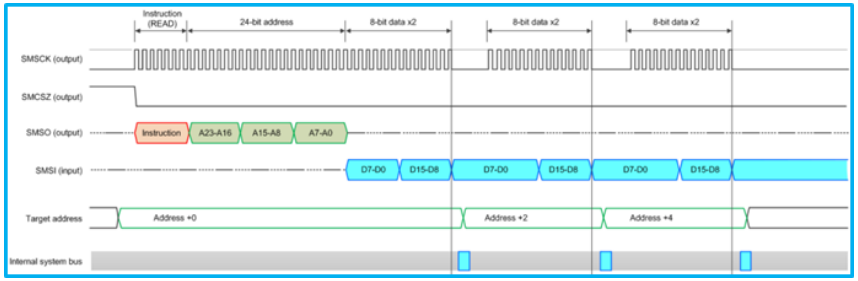
No. 139 12.4.4 (2) ROM Reading by Using Prefetching

[Figure 12.15 Continuous Data Reading by Using Prefetching] added.

V8.00		V9.00	
Page	Description	Page	Description
12-21	**[12.4.4 (2) ROM reading by using prefetching]** *(No entry)*	12-22	**[12.4.4 (2) ROM Reading by Using Prefetching]** [Figure 12.15 Continuous Data Reading by Using Prefetching] 

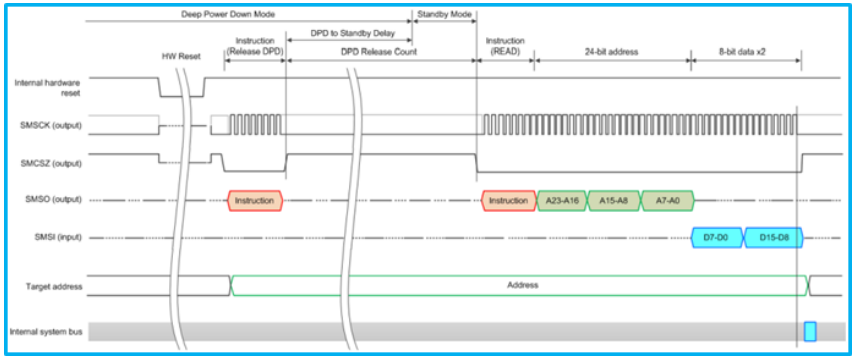
No. 140 12.4.4 (4) ROM Reading by Using SPI Bus Cycle Extension

[Figure 12.16 Continuous Data Reading by Using SPI Bus Cycle Extension] added.

V8.00		V9.00	
Page	Description	Page	Description
12-22	**[12.4.4 (4) ROM reading by using SPI bus cycle extension]** *(No entry)*	12-23	**[12.4.4 (4) ROM Reading by Using SPI Bus Cycle Extension]** [Figure 12.16 Continuous Data Reading by Using SPI Bus Cycle Extension] 

No. 141 12.4.5 Automatic Release from the Deep Power-Down State

[Figure 12.17 Operation for Automatic Release from the Deep Power-Down State] added.

V8.00		V9.00	
Page	Description	Page	Description
12-23	**[12.4.5 Automatic Release from the Deep Power-Down State]** *(No entry)*	12-24	**[12.4.5 Automatic Release from the Deep Power-Down State]** [Figure 12.17 Operation for Automatic Release from the Deep Power-Down State] 

No. 142 12.4.6 (3) SPI Bus Cycle Generation in Direct Communications Mode

Caution 2 added.

V8.00		V9.00	
Page	Description	Page	Description
12-24	**[12.4.6 (3) SPI bus cycle generation in direct communications mode]** *(No entry)*	12-25	**[12.4.6 (3) SPI Bus Cycle Generation in Direct Communications Mode]** Caution 2. The completion of an SPI bus cycle by writing to a register other than SFMCMD is not guaranteed as official functionality.

No. 143 13.1.1 Overview

Caution 2 added.

V8.00		V9.00	
Page	Description	Page	Description
13-4	**[13.1.1 Overview]** *(No entry)*	13-4	**[13.1.1 Overview]** Caution 2 ・The number of bytes for transfer must be divisible by 32 bits (= 1 word = 4 bytes).

No. 144 13.4.3.2 (4) (a) Channel status register (CHSTATn) (3/6)

Note modified.

V8.00		V9.00	
Page	Description	Page	Description
13-21	**[13.4.3.2 (4) (a) Channel status register (CHSTATn) (3/6)]** Note: A bus error occurs, for example, if an undefined area is accessed. This bit can be cleared to 0 by setting the CHCTRLn.SWRST bit to 1.	13-21	**[13.4.3.2 (4) (a) Channel status register (CHSTATn) (3/6)]** Note: If a reserved area in the memory map is specified as the destination for access, the internal bus (AHB) generates a bus error (address code error). This bit can be cleared to 0 by setting the CHCTRLn.SWRST bit to 1.

No. 145 13.4.3.2 (4) (b) Channel control register (CHCTRLn) (1/3)

Bit 14 SETSSWPRQ R/W attribute corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-25	**[13.4.3.2 (4) (b) Channel control register (CHCTRLn) (1/3)]** - R/W attribute: Bit 14 = 0	13-25	**[13.4.3.2 (4) (b) Channel control register (CHCTRLn) (1/3)]** - R/W attribute: Bit 14 = W

No. 146 13.4.3.2 (4) (c) Channel configuration register (CHCFGn) (5/7)

Caution added.

V8.00		V9.00	
Page	Description	Page	Description
13-32	**[13.4.3.2 (4) (c) Channel configuration register (CHCFGn) (5/7)]** [Bit Position 10 to 8: AM2-AM0] Caution: The settings of AM2 to AM0 may overlap those of the DMAIFCp register. In general, however, when the DMAACKZp signal is set to the level mode by using AM2 to AM0, the DMAIFCn register should use its initial values. Conversely, when the DMAIFCn register is used to extend the DMAACKZp pulse width or to use the DMAREQZp mask function, select the pulse mode by using AM2 to AM0.	13-32	**[13.4.3.2 (4) (c) Channel configuration register (CHCFGn) (5/7)]** [Bit Position 10 to 8: AM2-AM0] Cautions 1. The settings of AM2 to AM0 do not affect the actual operation while the interrupt request signal from on-chip peripheral modules and external interrupt input are selected. 2. The settings of AM2 to AM0 may duplicate those of the DMAIFCp register. In general, however, when the DMAACKZp signal is set to the level mode by using AM2 to AM0, the DMAIFCn register should be left at its initial value. Conversely, when the DMAIFCn register is used to extend the DMAACKZp pulse width or for the DMAREQZp mask function, set AM2 to AM0 to select the pulse mode.

No. 147 13.4.4.2 (4) (b) Channel control register (RTCHCTRL) (1/3)

Bit 14 SETSSWPRQ R/W attribute corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-59	**[13.4.4.2 (4) (b) Channel control register (RTCHCTRL) (1/3)]** - R/W attribute: Bit 14 = 0	13-58	**[13.4.4.2 (4) (b) Channel control register (RTCHCTRL) (1/3)]** - R/W attribute: Bit 14 = W

No. 148 13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)

Title of sub-section modified. Remark added.

V8.00		V9.00	
Page	Description	Page	Description
13-86	**[13.4.6 DMA Trigger Factor Selection Register (DTFRn, RTDTFR)]** *(No entry)*	13-84	**[13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)]** Remark: n = 0 to 3; p = 0, 1

No. 149 13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)

Name of interrupt corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-89	**[13.4.6 DMA Trigger Factor Selection Register (DTFRn, RTDTFR)]** [Bit Position 6 to 0: IFC6-IFC0] 78H: CC-Link RFSTB interrupt	13-87	**[13.4.6 DMA Trigger Source Selection Registers (DTFRn, RTDTFR)]** [Bit Position 6 to 0: IFC6-IFC0] 78H: CC-Link REFSTB interrupt

No. 150 13.7.2 (1) Register Mode Operation Flow

Remark corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-95	**[13.7.2 (1) Register mode operation flow]** Remark: n = 0-3	13-93	**[13.7.2 (1) Register Mode Operation Flow]** Remark: n = 0 to 3; p = 0, 1

No. 151 13.7.2 (2) (c) Terminal count output (DMATCZp) mask setting (CHCFGn.TCM)

Remark corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-96	**[13.7.2 (2) (c) Terminal count output (DMATCZp) mask setting (CHCFGn.TCM)]** Remark: n = 0-3	13-94	**[13.7.2 (2) (c) Terminal count output (DMATCZp) mask setting (CHCFGn.TCM)]** Remark: n = 0 to 3; p = 0, 1

No. 152 13.7.2 (3) (b) When two register sets are used for continuous execution

Remark corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-99	**[13.7.2 (3) (b) When two register sets are used for continuous execution]** Remark: n = 0-3	13-97	**[13.7.2 (3) (b) When two register sets are used for continuous execution]** Remark: n = 0 to 3; p = 0, 1

No. 153 13.8.3 (2) Edge detection

Register settings added to operation example, Remark deleted.

V8.00		V9.00	
Page	Description	Page	Description
13-120	**[13.8.3 (2) Edge detection]** [Figure 13.22 Edge Detection Mode Operation Example 1] DMA transfer request: Rising edge detection, request from the source. [Figure 13.23 Edge Detection Mode Operation Example 2] DMA transfer request: Rising edge detection, request from the destination Remark: n = 0-3	13-118	**[13.8.3 (2) Edge detection]** [Figure 13.22 Edge Detection Mode Operation Example 1] DMA transfer request: Rising edge detection Request from the source (CHCFGn.REQD = 0) [Figure 13.23 Edge Detection Mode Operation Example 2] DMA transfer request: Rising edge detection Request from the destination (CHCFGn.REQD = 1) *(No entry)*

No. 154 13.8.3 (3) Level detection

Register settings added to operation example, Remark deleted.

V8.00		V9.00	
Page	Description	Page	Description
13-121	**[13.8.3 (3) Level detection]** [Figure 13.24 Level Detection Mode Operation Example 1] DMA transfer request: High level detection, request from the source [Figure 13.25 Level Detection Mode Operation Example 2] DMA transfer request: High level detection, request from the destination. Remark: n = 0-3	13-119	**[13.8.3 (3) Level detection]** [Figure 13.24 Level Detection Mode Operation Example 1] DMA transfer request: High level detection Request from the source (CHCFGn.REQD = 0) [Figure 13.25 Level Detection Mode Operation Example 2] DMA transfer request: High level detection Request from the destination (CHCFGn.REQD = 1) Remark: n = 0 to 3; p = 0, 1

No. 155 13.8.4 (1) Specification of the acknowledge signal mode for each DMA transfer request source

Tables 13.27 and 13.28 corrected. Caution 2 modified.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>13-123</td><td>

[13.8.4 (1) Specification of the acknowledge signal mode for each DMA transfer request source]

[Table 13.27 Specification of the Acknowledge Signal Mode for Each DMA Transfer Request Source]

<table>
<tr><th>DMA transfer request source</th><th>DMA transfer request detection mode specification (CHCFGn.LVL, LEN, HEN)</th><th>DMA acknowledge signal specification (CHCFGn.AM2-AM0)</th></tr>
<tr><td>Interrupt request from an external pins (INTPZ0-INTPZ31)</td><td>To be set arbitrarily according to the specification of the DMA transfer request source.</td><td>Operation is not affected by any setting.</td></tr>
<tr><td>Interrupt request from internal peripheral function</td><td>Rising edge detection.</td><td>Operation is not affected by any setting.</td></tr>
<tr><td>DMA transfer request from an external pin (DMAREQZ0-DMAREQZ1)</td><td>To be set arbitrarily according to the specification of the DMA transfer request source.</td><td>To be set arbitrarily according to the specification of the DMA transfer request source.</td></tr>
</table>

[Table 13.28 DMA Acknowledge Signal (DMAACKZp) Output Mode]

<table>
<tr><th>AMn2</th><th>AMn1</th><th>AMn0</th><th>DMA acknowledge signal (DMAACKZp) output mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Pulse mode Note 1 (initial value)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>The active level is maintained until the DMA transfer request (DMAREQZp) becomes inactive.</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>Bus cycle mode Note 2
The active level is maintained during the DMA transfer bus cycle.</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>The output of the DMA acknowledge signal (DMAACKZp) is disabled.</td></tr>
</table>

Caution 2. The settings of the AM2 to AM0 bits may overlap those of the DMAIFCn register. In general, however, when the DMAACKZp signal operation is set to the level mode by using AM2 to AM0, the DMAIFCn register should use its initial values. Conversely, when the DMAIFCn register is used to extend the DMAACKZp pulse width or to use the DMAREQZp mask function, select the pulse mode by using AMn2 to AMn0.

Remark: n = 0-3

</td><td>13-121</td><td>

[13.8.4 (1) Specification of the acknowledge signal mode for each DMA transfer request source]

[Table 13.27 Specification of the Acknowledge Signal Mode for Each DMA Transfer Request Source]

<table>
<tr><th>DMA Transfer Request Source</th><th>DMA Transfer Request Detection Mode Specification (CHCFGn.LVL, LEN, HEN)</th><th>DMA Acknowledge Signal Specification (CHCFGn.AM2-AM0)</th></tr>
<tr><td>Interrupt request from external pins (INTPZ0-INTPZ31)</td><td>Rising edge detection.</td><td>The DMAACKZp and RTDMAACKZ pins cannot be used.</td></tr>
<tr><td>Interrupt request from internal peripheral modules</td><td>Rising edge detection.</td><td>The DMAACKZp and RTDMAACKZ pins cannot be used.</td></tr>
<tr><td>DMA transfer request from external pin (DMAREQZp, RTDMAREQZ)</td><td>To be set arbitrarily according to the specification of the DMA transfer request source.</td><td>To be set arbitrarily according to the specification of the DMA transfer request source.</td></tr>
</table>

[Table 13.28 DMA Acknowledge Signal (DMAACKZp) Output Mode]

<table>
<tr><th>AMn2</th><th>AMn1</th><th>AMn0</th><th>DMA Acknowledge Signal (DMAACKZp) Output Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Pulse mode Note1 (initial value)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Level mode
The active level is maintained until the DMA transfer request (DMAREQZp) becomes inactive.</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>Bus cycle mode Note2
The active level is maintained during the DMA transfer bus cycle.</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>The output of the DMA acknowledge signal (DMAACKZp) is disabled.</td></tr>
</table>

Caution 2. The settings of AM2 to AM0 may duplicate those of the DMAIFCn register. In general, however, when the DMAACKZp signal is set to the level mode by using AM2 to AM0, the DMAIFCn register should be left at its initial value. Conversely, when the DMAIFCn register is used to extend the DMAACKZp pulse width or for the DMAREQZp mask function, set AM2 to AM0 to select the pulse mode.

Remark: n = 0 to 3; p = 0, 1

</td></tr>
</table>

No. 156 13.8.4 (2) Pulse output

Register settings added to operation example, Remark corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-124	**[13.8.4 (2) Pulse output]** [Figure 13.26 Pulse Output Mode Operation Example 1] DMA transfer request: Rising edge detection, request from the source [Figure 13.27 Pulse Output Mode Operation Example 2] DMA transfer request: Rising edge detection, request from the destination. Remark: n = 0-3	13-122	**[13.8.4 (2) Pulse output]** [Figure 13.26 Pulse Output Mode Operation Example 1] DMA transfer request: Rising edge detection Request from the source (CHCFGn.REQD = 0) [Figure 13.27 Pulse Output Mode Operation Example 2] DMA transfer request: Rising edge detection Request from the destination (CHCFGn.REQD = 1) Remark: n = 0 to 3; p = 0, 1

No. 157 13.8.4 (3) Level output

Register settings added to operation example.

V8.00		V9.00	
Page	Description	Page	Description
13-125	**[13.8.4 (3) Level output]** [Figure 13.28 Level Output Mode Operation Example 1] DMA transfer request: High level detection, request from the source. [Figure 13.29 Level Output Mode Operation Example 2] DMA transfer request: High level detection, request from the destination	13-123	**[13.8.4 (3) Level output]** [Figure 13.28 Level Output Mode Operation Example 1] DMA transfer request: High level detection Request from the source (CHCFGn.REQD = 0) [Figure 13.29 Level Output Mode Operation Example 2] DMA transfer request: High level detection Request from the destination (CHCFGn.REQD = 1)

No. 158 13.8.4 (4) Bus cycle output

Register settings added to operation example.

V8.00		V9.00	
Page	Description	Page	Description
13-126	**[13.8.4 (4) Bus cycle output]** [Figure 13.30 Bus Cycle Output Mode Operation Example 1] DMA transfer request: Rising edge detection, request from the source [Figure 13.31 Bus Cycle Output Mode Operation Example 2] MA transfer request: High level detection, request from the destination	13-124	**[13.8.4 (4) Bus cycle output]** [Figure 13.30 Bus Cycle Output Mode Operation Example 1] DMA transfer request: Rising edge detection Request from the source (CHCFGn.REQD = 0) [Figure 13.31 Bus Cycle Output Mode Operation Example 2] DMA transfer request: High level detection Request from the destination (CHCFGn.REQD = 1)

No. 159 13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)

Signal names corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-139	**[13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)]** [Table 13.35 Channel Configuration Register (CHCFG_33) Settings of Setting Example 1] [Bit Position 29: RSW] 0: Does not invert RSEL3 after a DMA transaction (a series of DMA transfers) is completed. [Bit Position 26: RSEL] 0: Does not mask INTDMA when LV is set to 0 in link mode. [Bit Position 24: DEM] 0: Enables DMA INTDMA output when a DMA transaction is completed. [Bit Position 11: DRRP] 0: Stops the operation by setting the CHSTAT_33.DER bit to 1 when LV is set to 0 in link mode.	13-136	**[13.9.1 Setting Example 1 (Register Mode, Single Transfer Mode, and Hardware Trigger)]** [Table 13.35 Channel Configuration Register (CHCFG1) Settings of Setting Example 1] [Bit Position 29: RSW] 0: Does not invert RSEL after a DMA transaction (the series of DMA transfers) is completed. [Bit Position 26: RSEL] 0: Does not mask INTDERR0 when LV is set to 0 in link mode. [Bit Position 24: DEM] 0: Enables INTDMA01 output when a DMA transaction is completed. [Bit Position 11: DRRP] 0: Stops the operation by setting the CHSTAT1.DER bit to 1 when LV is set to 0 in link mode.

No. 160 13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)

Signal names corrected. Set value of bit 25 corrected. Description of bit 25 corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-142	**[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]** [Table 13.38 Channel Configuration Register (CHCFG_32) Settings of Setting Example 2] - Set value: Bit 25 = 0 [Bit Position 26: DIM] 0: Does not mask INTDMA when LV is set to 0 in link mode. [Bit Position 25: TCM] 0: Does not mask (enables terminal count output) [Bit Position 24: DEM] 0: Enables INTDMA output when a DMA transaction is completed. [Bit Position 11: DRRP] 0: Stops the operation by setting the CHSTAT.DER bit to 1 when LV is set to 0 in link mode.	13-139	**[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]** [Table 13.38 Channel Configuration Register (CHCFG2) Settings of Setting Example 2] - Set value: Bit 25 = 1 [Bit Position 26: DIM] 0: Does not mask INTDERR0 when LV is set to 0 in link mode. [Bit Position 25: TCM] 0: Masks terminal count output. [Bit Position 24: DEM] 0: Enables INTDMA02 output when a DMA transaction is completed. [Bit Position 11: DRRP] 0: Stops the operation by setting the CHSTAT2.DER bit to 1 when LV is set to 0 in link mode.

No. 161 13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)

Setting value corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-143	**[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]** [Figure 13.39 Operation Flow of Setting Example 2] CHCFG2 ← 1045 0402H	13-140	**[13.9.2 Setting Example 2 (Register Mode, Block Transfer Mode, and Software Trigger)]** [Figure 13.39 Operation Flow of Setting Example 2] CHCFG2 ← 1245 0402H

No. 162 13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)

Signal names corrected.

V8.00		V9.00	
Page	Description	Page	Description
13-145	**[13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)]** [Table 13.41 Channel Configuration Register (CHCFG_31) Settings of Setting Example 3] [Bit Position 30: REN] 1: Executes continuously (uses the Next register set selected by the RSEL1 bit). [Bit Position 26: DIM] 0: 0: Does not mask INTDMA when LV is set to 0 in link mode. [Bit Position 24: DEM] 1: Masks INTDMA output when a DMA transaction is completed. [Bit Position 11: DRRP] 0: Stops the operation by setting the CHSTAT.DER bit to 1 when LV is set to 0 in link mode.	13-142	**[13.9.3 Setting Example 3 (Register Mode: Continuous Execution, Block Transfer Mode, and Software Trigger)]** [Table 13.41 Channel Configuration Register (CHCFG1) Settings of Setting Example 3] [Bit Position 30: REN] 1: Executes continuously (uses the Next register set selected by the RSEL bit). [Bit Position 26: DIM] 0: Does not mask INTDERR0 when LV is set to 0 in link mode. [Bit Position 24: DEM] 1: Masks INTDMA01 output when a DMA transaction is completed. [Bit Position 11: DRRP] 0: Stops the operation by setting the CHSTAT1.DER bit to 1 when LV is set to 0 in link mode.

No. 163 14.1 Features of TAUJ2

Title of Sub-Section 14.1 modified.

V8.00		V9.00	
Page	Description	Page	Description
14-1	**[14.1 R-IN32M3 TAUJ2 Features]**	14-1	**[14.1 Features of TAUJ2]**

No. 164 14.1 Features of TAUJ2

Item “Clock supply” deleted.

V8.00		V9.00	
Page	Description	Page	Description
14-1	**[14.1 R-IN32M3 TAUJ2 Features]** Clock supply: Timer Array Units J provide one clock input.	14-1	**[14.1 Features of TAUJ2]** *(No entry)*

No. 165 14.1 Features of TAUJ2

[Table 14.1 TAUJ2 clock supply] deleted.

V8.00		V9.00	
Page	Description	Page	Description
14-1	**[14.1 R-IN32M3 TAUJ2 Features]** Table 14.1 TAUJ2 clock supply	14-1	**[14.1 Features of TAUJ2]** *(No entry)*

No. 166 14.1 Features of TAUJ2

Description of Interrupts and Peripherals updated.

V8.00		V9.00	
Page	Description	Page	Description
14-2	**[14.1 R-IN32M3 TAUJ2 Features]** Interrupts and Peripherals: The Interrupts and Peripheral Timer Array Unit can generate the following interrupt and DMA requests and Real-time Port trigger and Timer Capture trigger.	14-2	**[14.1 Features of TAUJ2]** Interrupts and Peripheral Modules: The following interrupt requests from TAUJ2 can be used as triggers for interrupt service routines or hardware ISRs (where listed as such), for DMA transfer (by the general-purpose DMAC or real-time port DMAC), for capture by a timer (TAUJ2), and for updating the real-time port pins (RP00-RP37).

No. 167 14.1 Features of TAUJ2

Title of [Table 14.3 TAUJ2 Interrupt Signals] expanded. Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
14-2	**[14.1 R-IN32M3 TAUJ2 Features]** [Table 14.3 TAUJ2 Interrupt Signals] *(Entry in the "Connected to" column for "INTTAUJ2I0")* ・DMA Controller trigger (DTFR/RTDFTR)	14-2	**[14.1 Features of TAUJ2]** [Table 14.2 TAUJ2 Interrupt Signals and Requests for Peripheral Modules] *(Entry in the "Connected to" column for "INTTAUJ2I0")* • DMA Controller trigger (DTFR/RTDTFR)

No. 168 14.1 Features of TAUJ2

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
14-2	**[14.1 R-IN32M3 TAUJ2 Features]** [Table 14.3 TAUJ2 Interrupt Signals] *(Entry in the "Connected to" column for "INTTAUJ2I1")* ・DMA Controller trigger (DTFR/RTDFTR)	14-2	**[14.1 Features of TAUJ2]** [Table 14.2 TAUJ2 Interrupt Signals and Requests for Peripheral Modules] *(Entry in the "Connected to" column for "INTTAUJ2I1")* • DMA Controller trigger (DTFR/RTDTFR)

No. 169 14.1 Features of TAUJ2

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
14-2	**[14.1 R-IN32M3 TAUJ2 Features]** [Table 14.3 TAUJ2 Interrupt Signals] *(Entry in the "Connected to" column for "INTTAUJ2I2")* ・DMA Controller trigger (DTFR/RTDFTR)	14-2	**[14.1 Features of TAUJ2]** [Table 14.2 TAUJ2 Interrupt Signals and Requests for Peripheral Modules] *(Entry in the "Connected to" column for "INTTAUJ2I2")* • DMA Controller trigger (DTFR/RTDTFR)

No. 170 14.1 Features of TAUJ2

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
14-2	**[14.1 R-IN32M3 TAUJ2 Features]** [Table 14.3 TAUJ2 Interrupt Signals] *(Entry in the "Connected to" column for "INTTAUJ2I3")* ・DMA Controller trigger (DTFR/RTDFTR)	14-2	**[14.1 Features of TAUJ2]** [Table 14.2 TAUJ2 Interrupt Signals and Requests for Peripheral Modules] *(Entry in the "Connected to" column for "INTTAUJ2I3")* • DMA Controller trigger (DTFR/RTDTFR)

No. 171 14.1 Features of TAUJ2

Caution added.

V8.00		V9.00	
Page	Description	Page	Description
14-2	**[14.1 R-IN32M3 TAUJ2 Features]** *(Below Table 14.3 TAUJ2 Interrupt Signals)* *(No entry)*	14-2	**[14.1 Features of TAUJ2]** *(Below Table 14.2 TAUJ2 Interrupt Signals and Requests for Peripheral Modules)* Caution: Since TINm and TOUTm are multiplexed on the same port pins, the input pin function for TINm must be set to a pin other than a port pin (m = 0 to 3). For details, see section 21.9.1, Timer Input Function Selection Register (SELCNT).

No. 172 14.3.2 (1) TAUJ2 Prescaler Clock Select Register (TAUJ2TPS)

Remark deleted.

V8.00		V9.00	
Page	Description	Page	Description
14-12	**[14.3.2 (1) TAUJ2TPS – TAUJ2 prescaler clock select register]** Remark: The TAUJ2 clock input PCLK is specified in the first section of this section under the keyword “Clock supply”.	14-12	**[14.3.2 (1) TAUJ2 Prescaler Clock Select Register (TAUJ2TPS)]** *(No entry)*

No. 173 14.3.3 (2) TAUJ2 Channel Counter Register (TAUJ2CNTm)

Note added.

V8.00		V9.00	
Page	Description	Page	Description
14-14	**[14.3.3 (2) TAUJ2CNTm – TAUJ2 channel counter register]** *(No entry)*	14-15	**[14.3.3 (2) TAUJ2 Channel Counter Register (TAUJ2CNTm)]** Note: The initial value depends on the operating mode set by the TAUJ2 channel mode OS register. The initial value is FFFF_FFFFH in interval timer mode or one-count mode and it is 0000_0000H in other modes. For details of the operating mode settings, see section14.3.3(3), TAUJ2 Channel Mode OS Register (TAUJ2CMORm).

No. 174 14.3.3 (3) TAUJ2 Channel Mode OS Register (TAUJ2CMORm)

Description of bits 4-0 modified.

V8.00		V9.00	
Page	Description	Page	Description
14-15	**[14.3.3 (3) TAUJ2CMORm – TAUJ2 channel mode OS register]** [Bit Position 4 to 0: TAUJ2MD[4:0]] Specifies the operation mode.	14-19	**[14.3.3 (3) TAUJ2 Channel Mode OS Register (TAUJ2CMORm)]** [Bit Position 4 to 0: TAUJ2MD[4:0]] Specifies the operating mode. Settings not listed in the following table are prohibited.

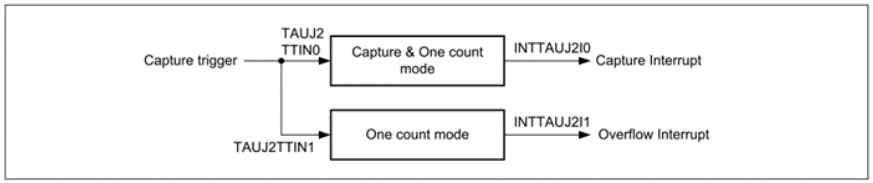
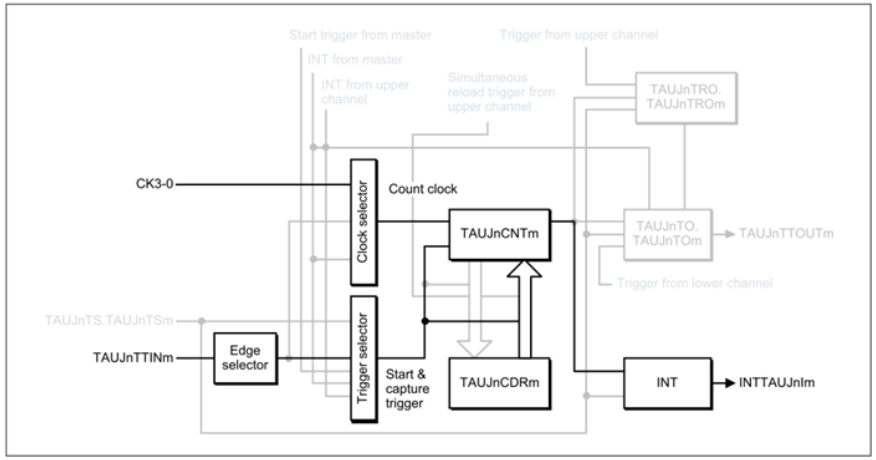
No. 175 14.5.1 Basic Rules of Synchronous Channel Operation

Description of synchronous channel operation modified.

V8.00		V9.00	
Page	Description	Page	Description
14-30	**[14.5.1 Basic rules of synchronous channel operation functions]** 4. If two master channels are used, slave channels cannot cross the master channels. Example: If CH0 and CH2 are master channels, CH1 can be set as a slave channel for CH0, but CH3 cannot.	14-31	**[14.5.1 Basic Rules of Synchronous Channel Operation]** 4. Multiple slave channels can be set for one master channel. Example: If CH0 is a master channel, CH1, CH2 and CH3 can be set as slave channels.

No. 176 14.7.5 (8) (b) Block diagram

Figure 14.24 replaced with more detailed version.

V8.00		V9.00	
Page	Description	Page	Description
14-69	**[14.7.5 (8) (b) Block diagram]** [Figure 14.24 Block diagram of overflow interrupt output (During TINn Width Measurement)]  	14-71	**[14.7.5 (8) (b) Block diagram]** [Figure 14.24 Block Diagram of Overflow Interrupt Output (for TAUJ2TTINm Width Measurement)] 

No. 177 15. Window Watchdog Timer A (WDTA)

Introductory description of Section 15 modified.

V8.00		V9.00	
Page	Description	Page	Description
15-1	**[15. Window Watchdog Timer A (WDTA)]** This section contains a generic description of window watchdog timer A. Section 15.1 describe all properties specific to the R-IN32M3, such as the number of channels, register base addresses, and input/output signal names. The subsequent sections describe the features that apply to all implementations Usage notes are given in section 15.6, Notes.	15-1	**[15. Window Watchdog Timer A (WDTA)]** This section explains window watchdog timer A.

No. 178 15.1 Features of WDTA

Title of Section 15.1 modified. Item “Clock supply” deleted. [Table 15.2 Clock Signal of Window Watchdog Timer A] removed.

V8.00		V9.00	
Page	Description	Page	Description
15-1	**[15.1 R-IN32M3 WDTA Features]** ・Clock supply The input clock for window watchdog timer A is WDTATCKI. WDTATCKI is connected to a clock generator. Table 15.2 Clock Signal of Window Watchdog Timer A	15-1	**[15.1 Features of WDTA]** *(No entry)* *(No entry)*

No. 179 15.2 Functional Overview

Description of Overflow time modified.

V8.00		V9.00	
Page	Description	Page	Description
15-2	**[15.2 Functional Overview]** • Overflow Time - 25 MHz: 163 µs to 5.36 s	15-2	**[15.2 Functional Overview]** • Overflow Time - 163 µs to 5.36 s

No. 180 16. Asynchronous Serial Interface J (UARTJ)

Title and introductory description of Section 16 modified.

V8.00		V9.00	
Page	Description	Page	Description
16-1	**[16. Asynchronous Serial Interface J (UARTJn)]** This section contains a generic description of asynchronous serial interface J.	16-1	**[16. Asynchronous Serial Interface J (UARTJ)** This section explains asynchronous serial interface J (UARTJ).

No. 181 16.1 Features of UARTJn

Title of Sub-Section 16.1 modified.

V8.00		V9.00	
Page	Description	Page	Description
16-1	**[16.1 R-IN32M3 UARTJn Features]**	16-1	**[16.1 Features of UARTJn]**

No. 182 16.1 Features of UARTJn

Item “Clock supply” and [Table 16.2 UARTJn clock supply] deleted.

V8.00		V9.00	
Page	Description	Page	Description
16-1	**[16.1 R-IN32M3 UARTJn Features]** • Clock supply: All UARTJn provide one clock input. It is connected to PCLK. Table 16.2 UARTJn clock supply	16-1	**[16.1 Features of UARTJn]** *(No entry)* *(No entry)*

No. 183 16.1 Features of UARTJn

Name of item “Interrupts” and its description expanded.

V8.00		V9.00	
Page	Description	Page	Description
16-2	**[16.1 R-IN32M3 UARTJn Features]** • Interrupts: The interrupts of the asynchronous serial interface J are listed in the table below.	16-2	**[16.1 Features of UARTJn]** • Interrupts and peripheral modules: The following interrupt requests from UARTJ can be used as triggers for interrupt service routines or hardware ISRs (where listed as such), for DMA transfer (by the general-purpose DMAC or real-time port DMAC), for capture by a timer (TAUJ2), and for updating the real-time port pins (RP00-RP37).

No. 184 16.1 Features of UARTJn

Signal names in table corrected.

V8.00		V9.00	
Page	Description	Page	Description
16-2	**[16.1 R-IN32M3 UARTJn Features]** [Table 16.4 UARTJn interrupts] • UARTJn signals: INTUAJ0TIT Function: Transmission interrupt Connected to: DMA controller trigger (DTFR/RTDFTR) • UARTJn signals: INTUAJ0TIR Function: Reception interrupt Connected to: DMA controller trigger (DTFR/RTDFTR)) • UARTJn signals: INTUAJ1TIT Function: Transmission interrupt Connected to: DMA controller trigger (DTFR/RTDFTR) • UARTJn signals: INTUAJ1TIR Function: Reception interrupt Connected to: DMA controller trigger (DTFR/RTDFTR)	16-2	**[16.1 Features of UARTJn]** [Table 16.3 UARTJn Interrupts] • UARTJn signals: INTUAJ0TIT Function: Transmission interrupt Connected to: DMA controller trigger (DTFR/RTDTFR) • UARTJn signals: INTUAJ0TIR Function: Reception interrupt Connected to: DMA controller trigger (DTFR/RTDTFR) • UARTJn signals: INTUAJ1TIT Function: Transmission interrupt Connected to: DMA controller trigger (DTFR/RTDTFR) • UARTJn signals: INTUAJ1TIR Function: Reception interrupt Connected to: DMA controller trigger (DTFR/RTDTFR)

No. 185 16.4 (2) UARTJn control register 1 (URTJnCTL1)

Value in description of bits 14-12 corrected.

V8.00		V9.00	
Page	Description	Page	Description
16-9	**[16.4 (2) URTJnCTL1 — UARTJn control register 1]** [Bit Position 14 to 12: URTJnBLG[2:0]] BF bit length during transmission 110: 15 bits	16-9	**[16.4 (2) UARTJn control register 1 (URTJnCTL1)]** [Bit Position 14 to 12: URTJnBLG[2:0]] BF bit length during transmission 111: 15 bits

No. 186 16.4 (5) UARTJn status register 0 (URTJnSTR0)

Notes 1 and 2 added.

V8.00		V9.00	
Page	Description	Page	Description
16-15	**[16.4 (5) URTJnSTR0 — UARTJn status register 0]** *(No entry)*	16-15	**[16.4 (5) UARTJn status register 0 (URTJnSTR0)]** Notes 1. This bit is also initialized when reception is disabled by setting URTJnCTL0.URTJnRXE = 0. 2. These bits are also initialized when transmission is disabled by setting URTJnCTL0.URTJnTXE = 0.

No. 187 16.4 (6) UARTJn status register 1 (URTJnSTR1)

Notes 1 and 2 added.

V8.00		V9.00	
Page	Description	Page	Description
16-16	**[16.4 (6) URTJnSTR1 — UARTJn status register 1]** *(No entry)*	16-16	**[16.4 (6) UARTJn status register 1 (URTJnSTR1)]** Notes 1. This bit is also initialized when reception is disabled by setting URTJnCTL0.URTJnRXE = 0. 2. This bit is also initialized when transmission is disabled by setting URTJnCTL0.URTJnTXE = 0.

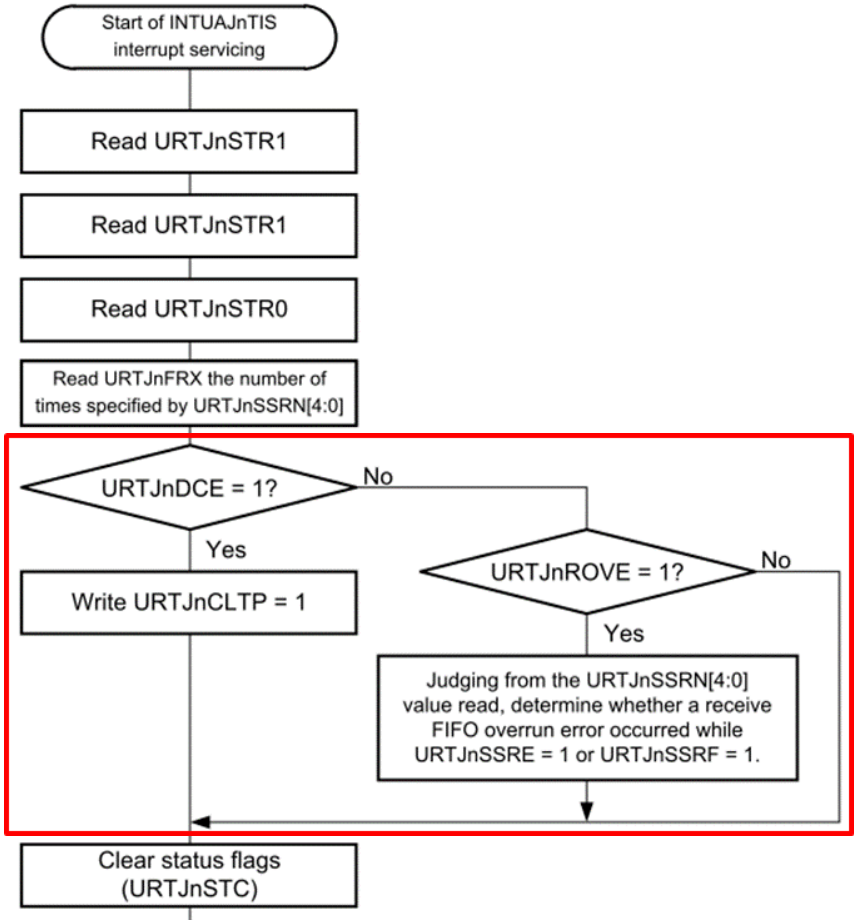
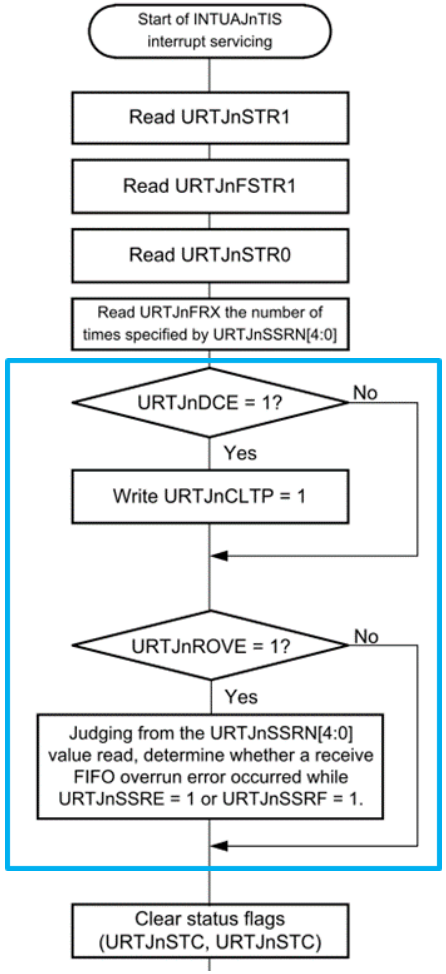
No. 188 16.4 (6) UARTJn status register 1 (URTJnSTR1)

Note 1 added.

V8.00		V9.00	
Page	Description	Page	Description
16-17	**[16.4 (6) URTJnSTR1 — UARTJn status register 1]** *(No entry)*	16-17	**[16.4 (6) UARTJn status register 1 (URTJnSTR1)]** Note 1. This bit is also initialized when reception is disabled by setting URTJnCTL0.URTJnRXE = 0.

No. 189 16.5.3 Status Interrupt Request INTUAJnTIS

Flow chart corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>16-31</td><td>[16.5.3 Status interrupt request INTUAJnTIS]
[Figure 16.4 Processing flow after interrupt generation]
 
</td><td>16-31</td><td>[16.5.3 Status Interrupt Request INTUAJnTIS]
[Figure 16.4 Processing Flow after Interrupt Generation]
 
</td></tr>
</table>

No. 190 16.6.6 (2) Reception start and stop

Supplement c) added to Figure 16.15.

V8.00		V9.00	
Page	Description	Page	Description
16-46	**[16.6.6 (2) Reception start and stop]** [Figure 16.15 Flowchart of data reception when URTJnSLBM = 0, URTJnSSBR = 1] *(No entry)*	16-46	**[16.6.6 (2) Reception start and stop]** [Figure 16.15 Flowchart of Data Reception when URTJnSLBM = 0, URTJnSSBR = 1] c) Set the pointer value to receive data following BF reception.

No. 191 16.7 Bit-Rate Generator

Title of Sub-Section 16.7 corrected. Equation for the calculation of Bit rate added. Table 16.8 added. Remarks and Note added.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>16-52</td><td>[16.7 Baud Rate Generator]
(No entry)</td><td>16-54</td><td>[16.7 Bit-Rate Generator]
The clock setting for the bit rate is calculated from the following formula. For details of the register, see section 16.4(3), UARTJn control register 2 (URTJnCTL2).
$$\text{Bit rate} = \frac{\text{PCLK frequency}}{2\times(\text{URTJnCTL2.URTJnBRS11}-0)\times 2^{\text{URTJnCTL2.URTJnPRS2}-0}} = \text{BRT[bps]}$$
$$\text{Error in the bit rate} = \left\{\frac{\text{Bit rate (BRT)}}{\text{Target bit rate (target BRT)}} - 1\right\}\times 100 = \text{ERR[\%]}$$
Remark: The settings of the register when the bit rate is set to 2.94 Mbps are as follows (decimal notation).
URTJnCTL2.URTJnBRS = 2125
URTJnCTL2.URTJnRRS = 3
Table 16.8 Allowable Scope of Error in Bit Rate
<table><tr><th>URTJnCTL2.URTJnBRS[11:0] (decimal notation) Note</th><th>Maximum Bit Rate</th><th>Minimum Bit Rate</th></tr><tr><td>4</td><td>+ 2.32%</td><td>- 2.43%</td></tr><tr><td>8</td><td>+ 3.52%</td><td>- 3.61%</td></tr><tr><td>16</td><td>+ 4.14%</td><td>- 4.19%</td></tr><tr><td>32</td><td>+ 4.45%</td><td>- 4.47%</td></tr><tr><td>64</td><td>+ 4.60%</td><td>- 4.62%</td></tr><tr><td>128</td><td>+ 4.68%</td><td>- 4.69%</td></tr><tr><td>256</td><td>+ 4.72%</td><td>- 4.72%</td></tr><tr><td>512</td><td>+ 4.74%</td><td>- 4.74%</td></tr><tr><td>1024</td><td>+ 4.75%</td><td>- 4.75%</td></tr><tr><td>2048</td><td>+ 4.75%</td><td>- 4.75%</td></tr><tr><td>4095</td><td>+ 4.75%</td><td>- 4.75%</td></tr></table>Note: When the setting of URTJnCTL2.URTJnBRS[11:0] is 0 to 3, refer to the entry for 4.
Remark: When URTJnCTL2.URTJnBRS[11:0] = “2125”, the allowable scope of error in the bit rate error is ±4.75%.</td></tr>
</table>

No. 192 17. Clocked Serial Interface H (CSIH)

Introductory description of Section 17 modified.

V8.00		V9.00	
Page	Description	Page	Description
17-1	**[17. Clocked Serial Interface H (CSIH)]** This section contains a generic description of clocked serial interface H (CSIH). The first part in this section describes the features specific to an R-IN32M3, including the channels, register base addresses, and input/output signal names. The remainder of the section describes the features that apply to all implementations.	17-1	**[17. Clocked Serial Interface H (CSIH)]** This section explains clocked serial interface H (CSIH).

No. 193 17.1 Features of CSIH

Title of Sub-Section 17.1 modified.

V8.00		V9.00	
Page	Description	Page	Description
17-1	**[17.1 Features of R-IN32M3 CSIH]**	17-1	**[17.1 Features of CSIH]**

No. 194 17.1 Features of CSIH

Item “Clock supply” deleted.

V8.00		V9.00	
Page	Description	Page	Description
17-1	**[17.1 Features of R-IN32M3 CSIH]** • Clock supply: Clocked serial interface H (CSIH) provide one clock input.	17-1	**[17.1 Features of CSIH]** *(No entry)*

No. 195 17.1 Features of CSIH

[Table 17.3 CSIHn Clock source] deleted.

V8.00		V9.00	
Page	Description	Page	Description
17-1	**[17.1 Features of R-IN32M3 CSIH]** Table 17.3 CSIHn Clock source	17-1	**[17.1 Features of CSIH]** *(No entry)*

No. 196 17.1 Features of CSIH

Title and description of item “Interrupts” expanded.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** • Interrupts: CSIH can generate the following interrupt, DMA requests, Timer Trigger and Real-time port trigger:	17-2	**[17.1 Features of CSIH]** • Interrupts and peripheral modules: The following interrupt requests from CSIH can be used as triggers for interrupt service routines or hardware ISRs (where listed as such), for DMA transfer (by the general-purpose DMAC or real-time port DMAC), for capture by a timer (TAUJ2), and for updating the real-time port pins (RP00-RP37).

No. 197 17.1 Features of CSIH

Title of [Table 17.5 CSIHn interrupt and DMA/DTS requests] modified.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** Table 17.5 CSIHn interrupt and DMA/DTS requests	17-2	**[17.1 Features of CSIH]** Table 17.4 CSIHn Interrupts and Requests to Peripheral Modules

No. 198 17.1 Features of CSIH

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** [Table 17.5 CSIHn interrupt and DMA/DTS requests] *(Entry in "Connected to" column for CSI0/CSIHTIC)* • DMA controller trigger (DTFR/RTDFTR)	17-2	**[17.1 Features of CSIH]** [Table 17.4 CSIHn Interrupts and Requests to Peripheral Modules] *(Entry in "Connected to" column for CSI0/CSIHTIC)* • DMA controller trigger (DTFR/RTDTFR)

No. 199 17.1 Features of CSIH

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** [Table 17.5 CSIHn interrupt and DMA/DTS requests] *(Entry in "Connected to" column for CSI0/CSIHTIR)* • DMA controller trigger (DTFR/RTDFTR)	17-2	**[17.1 Features of CSIH]** [Table 17.4 CSIHn Interrupts and Requests to Peripheral Modules] *(Entry in "Connected to" column for CSI0/CSIHTIR)* • DMA controller trigger (DTFR/RTDTFR)

No. 200 17.1 Features of CSIH

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** [Table 17.5 CSIHn interrupt and DMA/DTS requests] *(Entry in "Connected to" column for CSI0/CSIHTIJC)* • DMA controller trigger (DTFR/RTDFTR)	17-2	**[17.1 Features of CSIH]** [Table 17.4 CSIHn Interrupts and Requests to Peripheral Modules] *(Entry in "Connected to" column for CSI0/CSIHTIJC)* • DMA controller trigger (DTFR/RTDTFR)

No. 201 17.1 Features of CSIH

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** [Table 17.5 CSIHn interrupt and DMA/DTS requests] *(Entry in "Connected to" column for CSI1/CSIHTIC)* • DMA controller trigger (DTFR/RTDFTR)	17-2	**[17.1 Features of CSIH]** [Table 17.4 CSIHn Interrupts and Requests to Peripheral Modules] *(Entry in "Connected to" column for CSI1/CSIHTIC)* • DMA controller trigger (DTFR/RTDTFR)

No. 202 17.1 Features of CSIH

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** [Table 17.5 CSIHn interrupt and DMA/DTS requests] *(Entry in "Connected to" column for CSI1/CSIHTIR)* • DMA controller trigger (DTFR/RTDFTR)	17-2	**[17.1 Features of CSIH]** [Table 17.4 CSIHn Interrupts and Requests to Peripheral Modules] *(Entry in "Connected to" column for CSI1/CSIHTIR)* • DMA controller trigger (DTFR/RTDTFR)

No. 203 17.1 Features of CSIH

Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-2	**[17.1 Features of R-IN32M3 CSIH]** [Table 17.5 CSIHn interrupt and DMA/DTS requests] *(Entry in "Connected to" column for CSI1/CSIHTIJC)* • DMA controller trigger (DTFR/RTDFTR)	17-2	**[17.1 Features of CSIH]** [Table 17.4 CSIHn Interrupts and Requests to Peripheral Modules] *(Entry in "Connected to" column for CSI1/CSIHTIJC)* • DMA controller trigger (DTFR/RTDTFR)

No. 204 17.3 (4) CSIH status register 0 (CSIHnSTR0)

Tables in the description of bit 7 corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>17-14</td><td>
[17.3 (4) CSIHnSTR0 — CSIH status register 0]
[Bit Position 7: CSIHnTSF]
<table>
<tr><th rowspan="2">Master mode</th><th colspan="3">Set condition</th></tr>
<tr><th>Direct access mode, FIFO mode</th><th>Dual buffer mode, Transmit only Buffer mode</th><th>Clear condition</th></tr>
<tr><td>Transmission mode</td><td rowspan="3">Writing to transmit data register</td><td rowspan="3">Setting CSIHnMCTL2. CSIHnBTST</td><td rowspan="3">Within 0.5 clock cycles from the last CSIHnTSCK edge</td></tr>
<tr><td>Transmission / reception mode</td></tr>
<tr><td>Reception mode</td></tr>
</table>
<table>
<tr><th rowspan="2">Slave mode</th><th colspan="3">Set condition</th></tr>
<tr><th>Direct access mode, FIFO mode</th><th>Dual buffer mode, Transmit only Buffer mode</th><th>Clear condition</th></tr>
<tr><td>Transmission mode</td><td rowspan="2">Writing to transmit data register</td><td rowspan="3">Setting CSIHnMCTL2. CSIHnBTST</td><td rowspan="3">Within 0.5 clock cycles from the last CSIHnTSCK edge</td></tr>
<tr><td>Transmission / reception mode</td></tr>
<tr><td>Reception mode</td><td>CSIHnTSCK input timing</td></tr>
</table>
</td><td>17-14</td><td>
[17.3 (4) CSIH status register 0 (CSIHnSTR0)]
[Bit Position 7: CSIHnTSF]
<table>
<tr><th rowspan="2">Master Mode</th><th colspan="3">Setting Condition</th></tr>
<tr><th>Direct Access Mode, FIFO Mode</th><th>Dual Buffer Mode, Transmit Only Buffer Mode</th><th>Clearing Condition</th></tr>
<tr><td>Transmission mode</td><td rowspan="3">Writing to transmit data register</td><td rowspan="3">Setting CSIHnMCTL2. CSIHnBTST</td><td rowspan="3">Within 0.5 clock cycles from the last CSIHnTSCK edge</td></tr>
<tr><td>Transmission / reception mode</td></tr>
<tr><td>Reception mode</td></tr>
</table>
<table>
<tr><th rowspan="2">Slave Mode</th><th colspan="3">Setting Condition</th></tr>
<tr><th>Direct Access Mode, FIFO Mode</th><th>Dual Buffer Mode, Transmit Only Buffer Mode</th><th>Clearing Condition</th></tr>
<tr><td>Transmission mode</td><td rowspan="2">Writing to transmit data register</td><td rowspan="3">Setting CSIHnMCTL2. CSIHnBTST</td><td rowspan="3">Within 0.5 clock cycles from the last CSIHnTSCK edge</td></tr>
<tr><td>Transmission / reception mode</td></tr>
<tr><td>Reception mode</td><td>CSIHnTSCK input timing</td></tr>
</table>
</td></tr>
</table>

No. 205 17.3 (4) CSIH status register 0 (CSIHnSTR0)

Remark added.

V8.00		V9.00	
Page	Description	Page	Description
17-16	**[17.3 (4) CSIHnSTR0 — CSIH status register 0]** [Table 17.9 Memory mode operation] *(No entry)*	17-16	**[17.3 (4) CSIH status register 0 (CSIHnSTR0)]** [Table 17.8 Memory Mode Operation] Remark: n = 0, 1

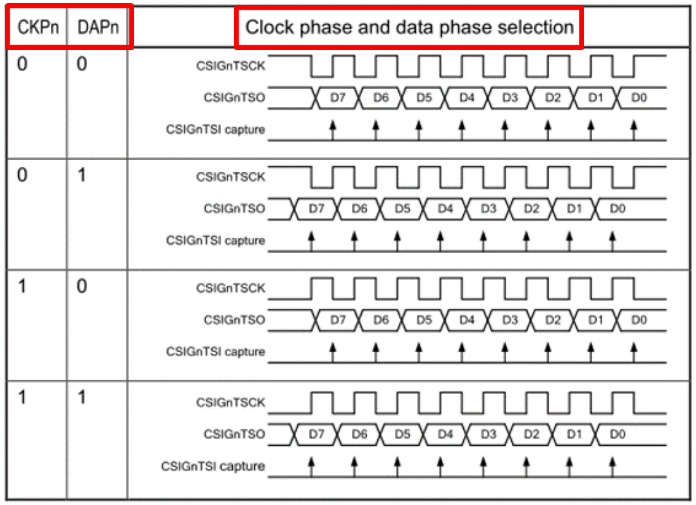
No. 206 17.3 (6) CSIH memory control register 0 (CSIHnMCTL0)

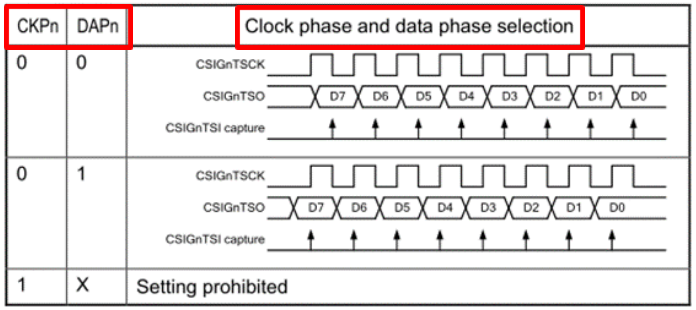
Description of bits 4-0 modified.

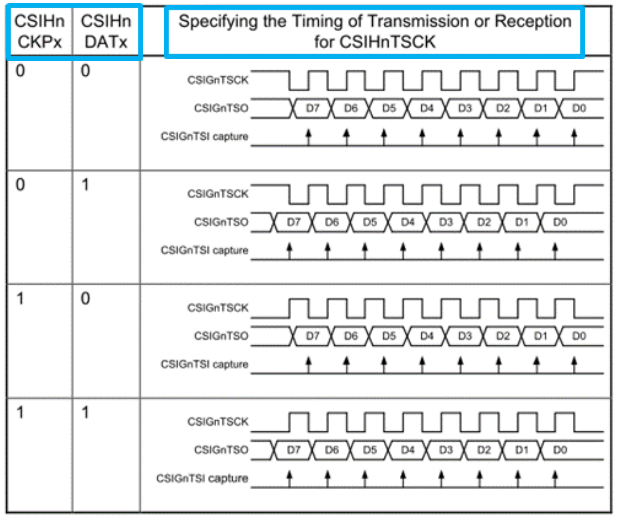
V8.00		V9.00	
Page	Description	Page	Description
17-19	**[17.3 (6) CSIHnMCTL0 — CSIH Memory control register 0]** [Bit Position 4 to 0: CSIHnTO [4:0]] Select the FIFO mode timeout setting.	17-19	**[17.3 (6) CSIH memory control register 0 (CSIHnMCTL0)]** [Bit Position 4 to 0: CSIHnTO [4:0]] Select the number of clock cycles until the timeout is reached.

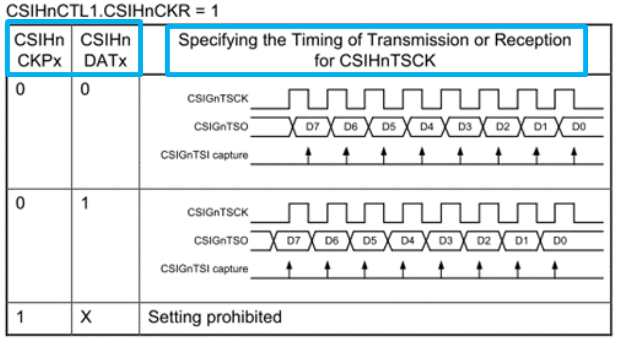
No. 207 17.3 (10) CSIH configuration register x (CSIHnCFGx)

Names of bits and titles of tables in the description of bits 17-16 corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>17-27</td><td>
[17.3 (10) CSIHnCFGx — CSIH configuration register x]
[Bit Position 17, 16: CSIHnCKPx, CSIHnDAPx]
CKP: Clock phase select bit
DAP: Data phase select bit
CSIHnCTL1.CSIHnCKR = 0


CSIHnCTL1.CSIHnCKR = 1


</td><td>17-27</td><td>
[17.3 (10) CSIH configuration register x (CSIHnCFGx)]
[Bit Position 17, 16: CSIHnCKPx, CSIHnDAPx]
CSIHnCKPx: Clock phase select bit
CSIHnDATx: Data phase select bit
CSIHnCTL1.CSIHnCKR = 0


CSIHnCTL1.CSIHnCKR = 1


</td></tr>
</table>

No. 208 17.3 (10) CSIH configuration register x (CSIHnCFGx)

Table in the description of bits 14-12 expanded.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>17-28</td><td>[17.3 (10) CSIHnCFGx — CSIH configuration register x]
[Bit Position 14 to 12: CSIHnIDx[2:0]]
<table><tr><th>CSIHnIDx[2:0]</th><th>Idle timing</th></tr><tr><td>000B</td><td>0.5 transmission clock cycles</td></tr><tr><td>001B</td><td>1.0 transmission clock cycles</td></tr><tr><td>010B</td><td>1.5 transmission clock cycles</td></tr><tr><td>...</td><td>... (2.5, 3.5, 4.5, 6.5)</td></tr><tr><td>111B</td><td>8.5 transmission clock cycles</td></tr></table></td><td>17-28</td><td>[17.3 (10) CSIH configuration register x (CSIHnCFGx)]
[Bit Position 14 to 12: CSIHnIDx[2:0]]
<table><tr><th>CSIHnIDx[2:0]</th><th>Idle Timing</th></tr><tr><td>000B</td><td>0.5 transmission clock cycles</td></tr><tr><td>001B</td><td>1.0 transmission clock cycles</td></tr><tr><td>010B</td><td>1.5 transmission clock cycles</td></tr><tr><td>011B</td><td>2.5 transmission clock cycles</td></tr><tr><td>100B</td><td>3.5 transmission clock cycles</td></tr><tr><td>101B</td><td>4.5 transmission clock cycles</td></tr><tr><td>110B</td><td>6.5 transmission clock cycles</td></tr><tr><td>111B</td><td>8.5 transmission clock cycles</td></tr></table></td></tr>
</table>

No. 209 17.3 (10) CSIH configuration register x (CSIHnCFGx)

Table in the description of bits 11-8 expanded.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>17-28</td><td>
[17.3 (10) CSIHnCFGx — CSIH configuration register x]
[Bit Position 11 to 8: CSIHnHDx[3:0]]
<table>
<tr><th>CSIHnHDx [3:0]</th><th>Hold timing with CSIHnCTL1.CSIHnSIT = 0</th><th>Hold timing with CSIHnCTL1.CSIHnSIT = 1</th></tr>
<tr><td>0000B</td><td>0.5 serial clock cycles</td><td>1.0 serial clock cycles</td></tr>
<tr><td>0001B</td><td>1 serial clock cycles</td><td>1.5 serial clock cycles</td></tr>
<tr><td>0010B</td><td>1.5 serial clock cycles</td><td>2.0 serial clock cycles</td></tr>
<tr><td>...</td><td>... (2.5, 3.5, 4.5, 6.5, 8.5, 9.5 10.5, 11.5, 12.5, 14.5, 16.5, 18.5)</td><td>... (3.0, 4.0, 5.0, 7.0, 9.0, 10.0, 11.0, 12.0, 13.0, 15.0, 17.0, 19.0)</td></tr>
<tr><td>1111B</td><td>20.5 serial clock cycles</td><td>21.0 serial clock cycles</td></tr>
</table>
</td><td>17-28</td><td>
[17.3 (10) CSIH configuration register x (CSIHnCFGx)]
[Bit Position 11 to 8: CSIHnHDx[3:0]]
<table>
<tr><th>CSIHnHDx [3:0]</th><th>Hold Timing with CSIHnCTL1.CSIHnSIT = 0</th><th>Hold Timing with CSIHnCTL1.CSIHnSIT = 1</th></tr>
<tr><td>0000B</td><td>0.5 serial clock cycles</td><td>1.0 serial clock cycles</td></tr>
<tr><td>0001B</td><td>1 serial clock cycles</td><td>1.5 serial clock cycles</td></tr>
<tr><td>0010B</td><td>1.5 serial clock cycles</td><td>2.0 serial clock cycles</td></tr>
<tr><td>0011B</td><td>2.5 serial clock cycles</td><td>3.0 serial clock cycles</td></tr>
<tr><td>0100B</td><td>3.5 serial clock cycles</td><td>4.0 serial clock cycles</td></tr>
<tr><td>0101B</td><td>4.5 serial clock cycles</td><td>5.0 serial clock cycles</td></tr>
<tr><td>0110B</td><td>6.5 serial clock cycles</td><td>7.0 serial clock cycles</td></tr>
<tr><td>0111B</td><td>8.5 serial clock cycles</td><td>9.0 serial clock cycles</td></tr>
<tr><td>1000B</td><td>9.5 serial clock cycles</td><td>10.0 serial clock cycles</td></tr>
<tr><td>1001B</td><td>10.5 serial clock cycles</td><td>11.0 serial clock cycles</td></tr>
<tr><td>1010B</td><td>11.5 serial clock cycles</td><td>12.0 serial clock cycles</td></tr>
<tr><td>1011B</td><td>12.5 serial clock cycles</td><td>13.0 serial clock cycles</td></tr>
<tr><td>1100B</td><td>14.5 serial clock cycles</td><td>15.0 serial clock cycles</td></tr>
<tr><td>1101B</td><td>16.5 serial clock cycles</td><td>17.0 serial clock cycles</td></tr>
<tr><td>1110B</td><td>18.5 serial clock cycles</td><td>19.0 serial clock cycles</td></tr>
<tr><td>1111B</td><td>20.5 serial clock cycles</td><td>21.0 serial clock cycles</td></tr>
</table>
</td></tr>
</table>

No. 210 17.3 (10) CSIH configuration register x (CSIHnCFGx)

Table in the description of bits 7-4 expanded.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>17-29</td><td>
[17.3 (10) CSIHnCFGx — CSIH configuration register x]
[Bit Position 7 to 4: CSIHnINx[3:0]]
<table>
<tr><th>CSIHnINx [3:0]</th><th>Inter-data time when CSIHnCTL1.CSIHnSIT = 0</th><th>Inter-data time when CSIHnCTL1.CSIHnSIT = 1</th></tr>
<tr><td>0000B</td><td>0.0 serial clock cycles</td><td>0.5 serial clock cycles</td></tr>
<tr><td>0001B</td><td>0.5 serial clock cycles</td><td>1.0 serial clock cycles</td></tr>
<tr><td>0010B</td><td>1.0 serial clock cycles</td><td>1.5 serial clock cycles</td></tr>
<tr><td>0011B</td><td>2.0 serial clock cycles</td><td>2.5 serial clock cycles</td></tr>
<tr><td>...</td><td>... (3.0, 4.0, 6.0, 8.0, 9.0, 10.0, 11.0, 12.0, 14.0, 16.0, 18.0)</td><td>... (3.5, 4.5, 6.5, 8.5, 9.5, 10.5, 11.5 12.5, 14.5, 16.5, 18.5)</td></tr>
<tr><td>1111B</td><td>20.0 serial clock cycles</td><td>20.5 serial clock cycles</td></tr>
</table>
</td><td>17-29</td><td>
[17.3 (10) CSIH configuration register x (CSIHnCFGx)]
[Bit Position 7 to 4: CSIHnINx[3:0]]
<table>
<tr><th>CSIHnINx [3:0]</th><th>Inter-Data Time when CSIHnCTL1.CSIHnSIT = 0</th><th>Inter-Data Time when CSIHnCTL1.CSIHnSIT = 1</th></tr>
<tr><td>0000B</td><td>0.0 serial clock cycles</td><td>0.5 serial clock cycles</td></tr>
<tr><td>0001B</td><td>0.5 serial clock cycles</td><td>1.0 serial clock cycles</td></tr>
<tr><td>0010B</td><td>1.0 serial clock cycles</td><td>1.5 serial clock cycles</td></tr>
<tr><td>0011B</td><td>2.0 serial clock cycles</td><td>2.5 serial clock cycles</td></tr>
<tr><td>0100B</td><td>3.0 serial clock cycles</td><td>3.5 serial clock cycles</td></tr>
<tr><td>0101B</td><td>4.0 serial clock cycles</td><td>4.5 serial clock cycles</td></tr>
<tr><td>0110B</td><td>6.0 serial clock cycles</td><td>6.5 serial clock cycles</td></tr>
<tr><td>0111B</td><td>8.0 serial clock cycles</td><td>8.5 serial clock cycles</td></tr>
<tr><td>1000B</td><td>9.0 serial clock cycles</td><td>9.5 serial clock cycles</td></tr>
<tr><td>1001B</td><td>10.0 serial clock cycles</td><td>10.5 serial clock cycles</td></tr>
<tr><td>1010B</td><td>11.0 serial clock cycles</td><td>11.5 serial clock cycles</td></tr>
<tr><td>1011B</td><td>12.0 serial clock cycles</td><td>12.5 serial clock cycles</td></tr>
<tr><td>1100B</td><td>14.0 serial clock cycles</td><td>14.5 serial clock cycles</td></tr>
<tr><td>1101B</td><td>16.0 serial clock cycles</td><td>16.5 serial clock cycles</td></tr>
<tr><td>1110B</td><td>18.0 serial clock cycles</td><td>18.5 serial clock cycles</td></tr>
<tr><td>1111B</td><td>20.0 serial clock cycles</td><td>20.5 serial clock cycles</td></tr>
</table>
</td></tr>
</table>

No. 211 17.3 (10) CSIH configuration register x (CSIHnCFGx)

Table in the description of bits 3-0 expanded.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>17-29</td><td>[17.3 (10) CSIHnCFGx — CSIH configuration register x]
[Bit Position 3 to 0: CSIHnSPx[3:0]]
<table><tr><th>CSIHnSPx [3:0]</th><th>Setup delay</th></tr><tr><td>0000B</td><td>0.5 serial clock cycles</td></tr><tr><td>0001B</td><td>1.0 serial clock cycles</td></tr><tr><td>0010B</td><td>1.5 serial clock cycles</td></tr><tr><td>...</td><td>... (2.5, 3.5, 4.5, 6.5, 8.5, 9.5 10.5, 11.5, 12.5, 14.5, 16.5, 18.5)</td></tr><tr><td>1111B</td><td>20.5 serial clock cycles</td></tr></table></td><td>17-29</td><td>[17.3 (10) CSIH configuration register x (CSIHnCFGx)]
[Bit Position 3 to 0: CSIHnSPx[3:0]]
<table><tr><th>CSIHnSPx[3:0]</th><th>Setup Delay</th></tr><tr><td>0000B</td><td>0.5 serial clock cycles</td></tr><tr><td>0001B</td><td>1.0 serial clock cycles</td></tr><tr><td>0010B</td><td>1.5 serial clock cycles</td></tr><tr><td>0011B</td><td>2.5 serial clock cycles</td></tr><tr><td>0100B</td><td>3.5 serial clock cycles</td></tr><tr><td>0101B</td><td>4.5 serial clock cycles</td></tr><tr><td>0110B</td><td>6.5 serial clock cycles</td></tr><tr><td>0111B</td><td>8.5 serial clock cycles</td></tr><tr><td>1000B</td><td>9.5 serial clock cycles</td></tr><tr><td>1001B</td><td>10.5 serial clock cycles</td></tr><tr><td>1010B</td><td>11.5 serial clock cycles</td></tr><tr><td>1011B</td><td>12.5 serial clock cycles</td></tr><tr><td>1100B</td><td>14.5 serial clock cycles</td></tr><tr><td>1101B</td><td>16.5 serial clock cycles</td></tr><tr><td>1110B</td><td>18.5 serial clock cycles</td></tr><tr><td>1111B</td><td>20.5 serial clock cycles</td></tr></table></td></tr>
</table>

No. 212 17.3 (14) CSIH receive data register 0 for half word access (CSIHnRX0H)

R/W attribute of bits 31-24 corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-34	**[17.3 (14) CSIHnRX0H — CSIH receive data register 0 for half word access]** - R/W attribute: Bit[31:24] = R/W	17-34	**[17.3 (14) CSIH receive data register 0 for half word access (CSIHnRX0H)]** - R/W attribute: Bit[31:24] = 0

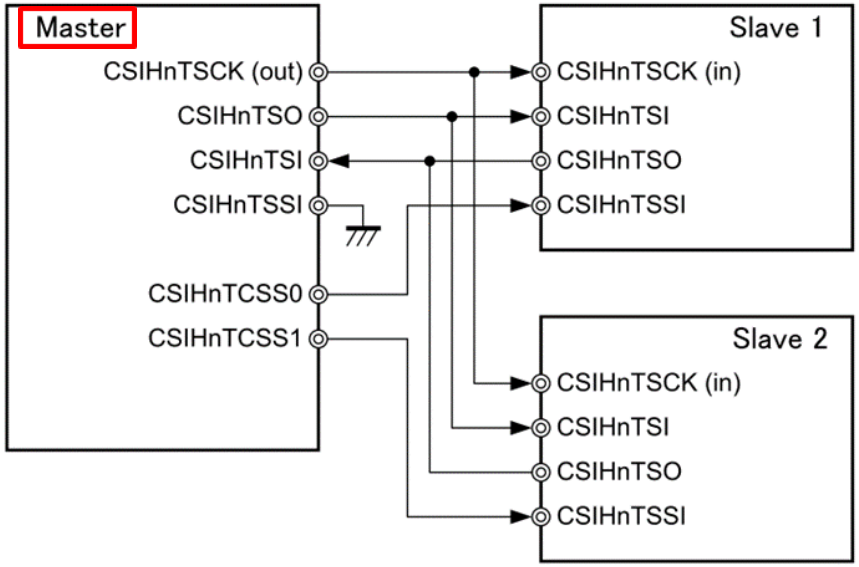
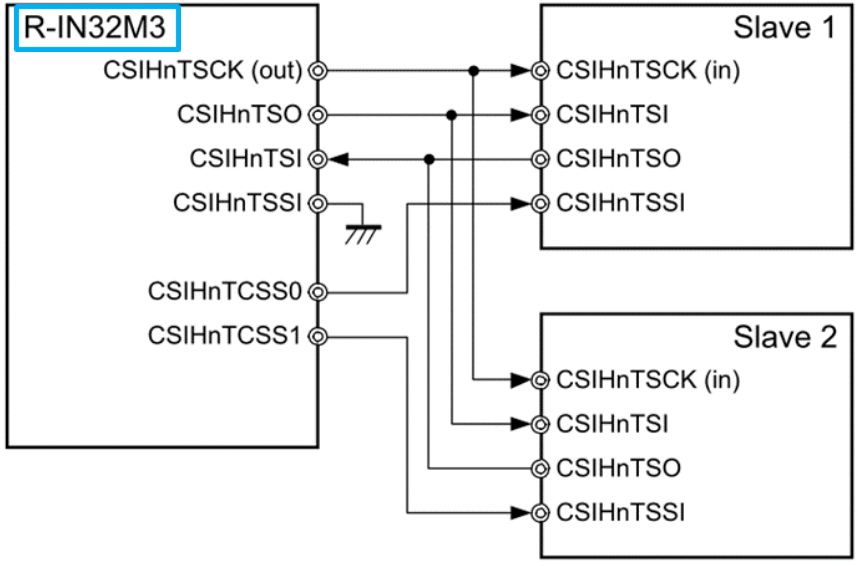
No. 213 17.4.2 (2) One master and two slaves

Title and description of Sub-Section 17.4.2 (2) modified.

V8.00		V9.00	
Page	Description	Page	Description
17-38	**[17.4.2 (2) One master and multiple slaves]** The following figure illustrates the connections between one master and multiple slaves. In this example, a configuration in which the master supplies one chip select (CS) signal to each slave is possible. This signal is connected to the slave select input CSIHnTSSI of the slave.	17-38	**[17.4.2 (2) One master and two slaves]** The following figure illustrates the connections between an R-IN32M3 as a master and two slaves. In this example, an R-IN32M3 can be configured to supply one chip select (CS) signal to each slave. This signal is connected to the slave select input CSIHnTSSI of the slave.

No. 214 17.4.2 (2) One master and two slaves

Titles of Sub-Section 17.4.2 (2) and Figure 17.5 modified. Labeling in Figure 17.5 modified.

V8.00		V9.00	
Page	Description	Page	Description
17-38	**[17.4.2 (2) One master and multiple slaves]** [Figure 17.5 Master to multiple slaves connection] 	17-38	**[17.4.2 (2) One master and two slaves]** [Figure 17.5 Connection between One Master and Two Slaves] 

No. 215 17.4.3 (1) Configuration registers

Description of Section 17.4.3 (1) corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-40	**[17.4.3 (1) Configuration registers]** Figure 17.6 "Chip select timings" shows an example in which the default active low setting is specified for the CS1 and CS2 signals (CSIHnCTL1.CSIHnCSL1 = 0, CSIHnCTL1.CSIHnCSL2 = 0). The active level can be separately specified for each CS.	17-40	**[17.4.3 (1) Configuration registers]** Figure 17.6 shows an example in which the default active low setting is specified for the CS0 and CS1 signals (CSIHnCTL1.CSIHnCSL0 = 0, CSIHnCTL1.CSIHnCSL1 = 0). The active level can be separately specified for each CS.

No. 216 17.4.14 Loop-Back Mode

Number of bits of CSIHnCTL1.CSIHnCLS corrected.

V8.00		V9.00	
Page	Description	Page	Description
17-78	**[17.4.14 Loop-back mode]** The CSIHnTSCK, CSIHnTSO, CSIHnTSI, and CSIHnTCSSn[7:0] signals are disconnected from ports. The CSIHnTSO signal is fixed to the low output level, and the CSIHnTSCK and CSIHnTCSSn[7:0] signals are set to the inactive level (the level specified for the CSIHnCFGx.CSIHnCKPx bit in the case of the CSIHnTSCK signal, and the level specified for the CSIHnCTL1.CSIHnCLS[7:0] bits in the case of the CSIHnTCSSn[7:0] signal).	17-75	**[17.4.14 Loop-Back Mode]** The CSIHnTSCK, CSIHnTSO, CSIHnTSI, and CSIHnTCSSn[7:0] signals are disconnected from ports. The CSIHnTSO signal is fixed to the low output level, and the CSIHnTSCK and CSIHnTCSSn[7:0] signals are set to the inactive level (the level specified by the CSIHnCFGx.CSIHnCKPx bit in the case of the CSIHnTSCK signal, and the level specified by the CSIHnCTL1.CSIHnCLS[1:0] bits in the case of the CSIHnTCSSn[7:0] signal).

No. 217 18. I2C BUS (IICB)

Introductory description of Section 18 modified.

V8.00		V9.00	
Page	Description	Page	Description
18-1	**[18. I2C BUS (IICB)]** Section 18.1 describes the features specific to an R-IN32M3, including the number of channels, register base addresses, and input/output signal names. Section 18.2 and subsequent sections describe the features that apply to all implementations.	18-1	**[18. I2C BUS (IICB)]** *(No entry)*

No. 218 18.1 Features of IICB

Title of Sub-Section 18.1 modified.

V8.00		V9.00	
Page	Description	Page	Description
18-1	**[18.1 Features of R-IN32M3 IICB]**	18-1	**[18.1 Features of IICB]**

No. 219 18.1 Features of IICB

Item “Clock supply” and [Table 18.2 IICBn clock supply] deleted.

V8.00		V9.00	
Page	Description	Page	Description
18-1	**[18.1 Features of R-IN32M3 IICB]** • Clock supply: IICBn uses PCLK as the clock input. PCLK is connected to the clock generator. Table 18.2 IICBn clock supply	18-1	**[18.1 Features of IICB]** *(No entry)* *(No entry)*

No. 220 18.1 Features of IICB

Title and description of item “Interrupt request signal” expanded.

V8.00		V9.00	
Page	Description	Page	Description
18-2	**[18.1 Features of R-IN32M3 IICB]** • Interrupt request signal: The IICBn uses a data transmit/receive interrupt request signal (IICBTIAn) and a status interrupt request signal (IICBTISn).	18-1	**[18.1 Features of IICB]** • Interrupts and peripheral modules: The following interrupt requests from IICB can be used as triggers for interrupt service routines or hardware ISRs (where listed as such), for DMA transfer (by the general-purpose DMAC or real-time port DMAC), for capture by a timer (TAUJ2), and for updating the real-time port pins (RP00-RP37).

No. 221 18.1 Features of IICB

Title of [Table 18.3 IICBn interrupt request signals] expanded. Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-2	**[18.1 Features of R-IN32M3 IICB]** [Table 18.3 IICBn interrupt request signals] [IICB0/IICBTIA, IICB1/IICBTIA] • DMA controller trigger (DTFR/RTDFTR)	18-1	**[18.1 Features of IICB]** [Table 18.2 IICBn Interrupts and Requests for Peripheral Modules] [IICB0/IICBTIA, IICB1/IICBTIA] • DMA controller trigger (DTFR/RTDTFR)

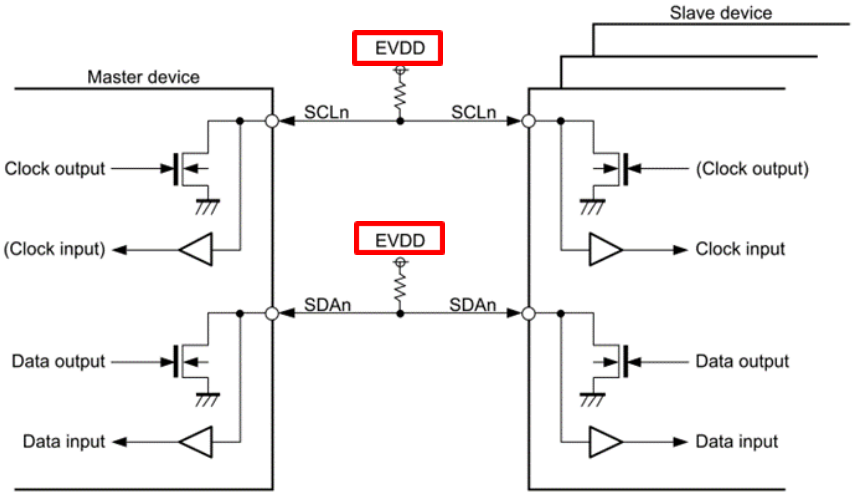
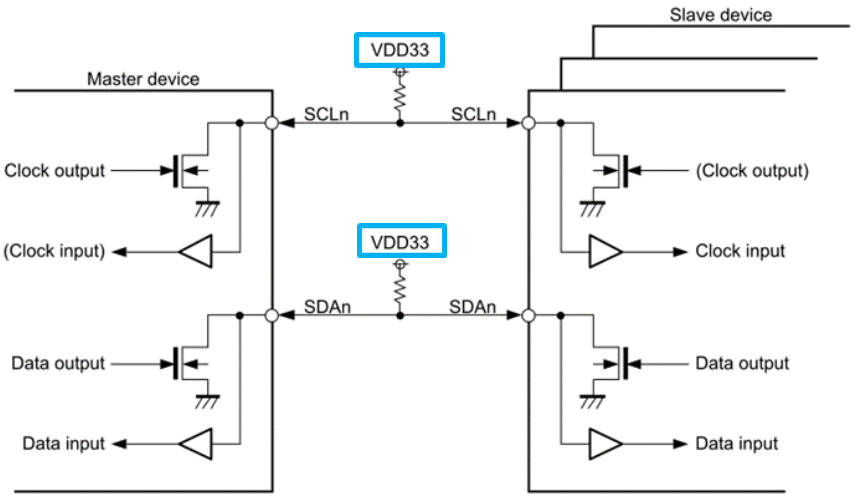
No. 222 18.3 (6) (a) Setting transfer clock by using IICBnWL and IICBnWH registers

Equation for Transfer clock corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-16	**[18.3 (6) (a) Setting transfer clock by using IICBnWL and IICBnWH registers]** Transfer clock (Hz) = PCLK/(IICBnWL + IICBnWH) + PCLK (t_R + t_F)	18-14	**[18.3 (6) (a) Setting transfer clock by using IICBnWL and IICBnWH registers]** $\text{Transfer clock (Hz)} = \frac{\text{PCLK}}{(\text{IICBnWL} + \text{IICBnWH}) + \text{PCLK}(t_R + t_F)}$ <R>

No. 223 18.4.1 Pin Configuration

Name of voltage source corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-32	**[18.4.1 Pin configuration]** [Figure 18.2 Pin configuration diagram] 	18-30	**[18.4.1 Pin Configuration]** [Figure 18.2 Pin Configuration Diagram] 

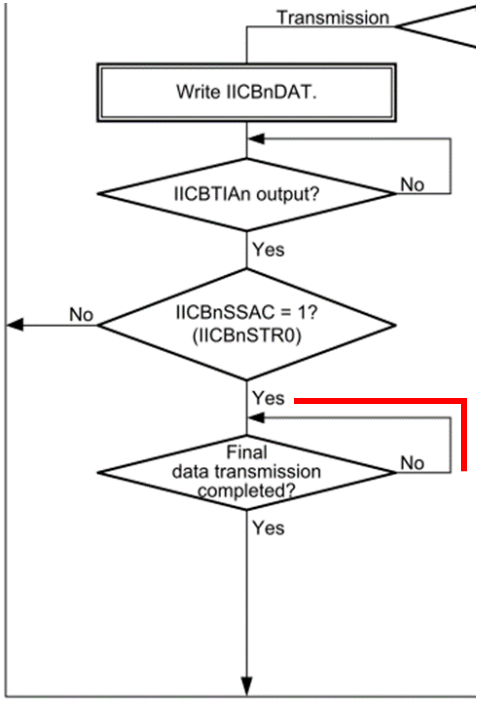
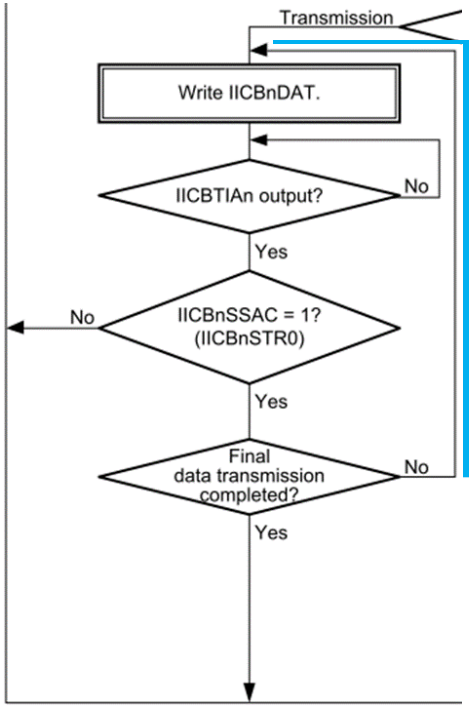
No. 224 18.6.1 (4) Example of communication in single transfer mode (slave transmission)

Remark added.

V8.00		V9.00	
Page	Description	Page	Description
18-44	**[18.6.1 (4) Example of communication in single transfer mode (slave transmission)]** *(No entry)*	18-42	**[18.6.1 (4) Example of communications in single transfer mode (slave transmission)]** Remark: During data transmission, set the IICBnCTL0.IICBnSLWT bit (to 1) so that the IICBn enters the wait state at the falling edge of the 9th clock.

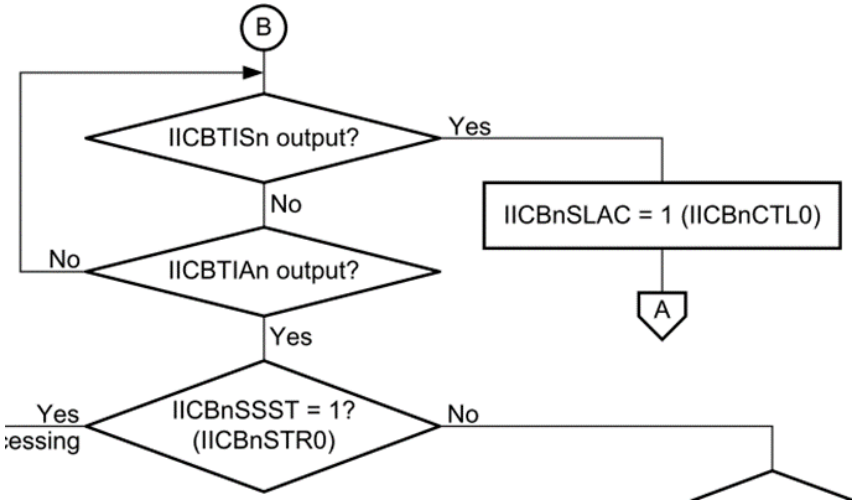
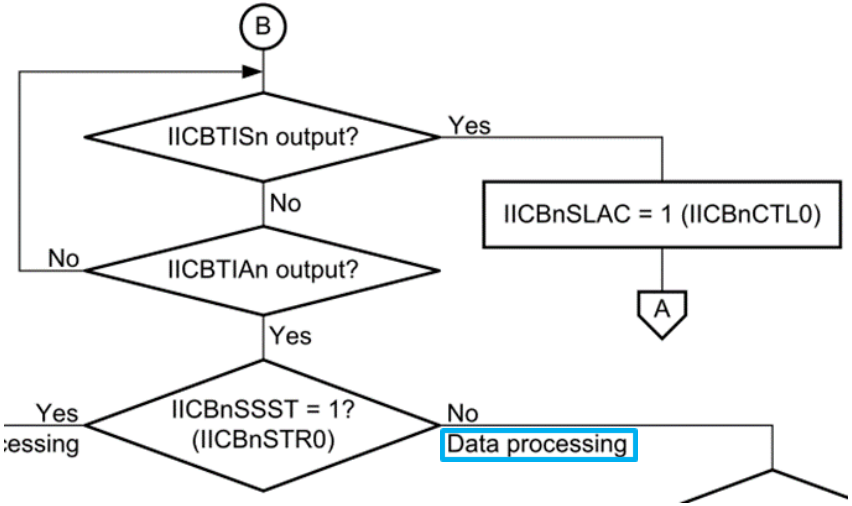
No. 225 18.9.1 (1) Master operation setting procedure during single transfer mode

Titles of Section 18.9.1 (1) and Figure 18.14 modified. Branch destination corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-118	**[18.9.1 (1) Master operate setting sequence during single transfer mode]** [Figure 18.14 Master operate setting sequence during single transfer mode (single master environment)] 	18-117	**[18.9.1 (1) Master operation setting procedure during single transfer mode]** [Figure 18.14 Master Operation Setting Procedure during Single Transfer Mode (Single Master Environment)] 

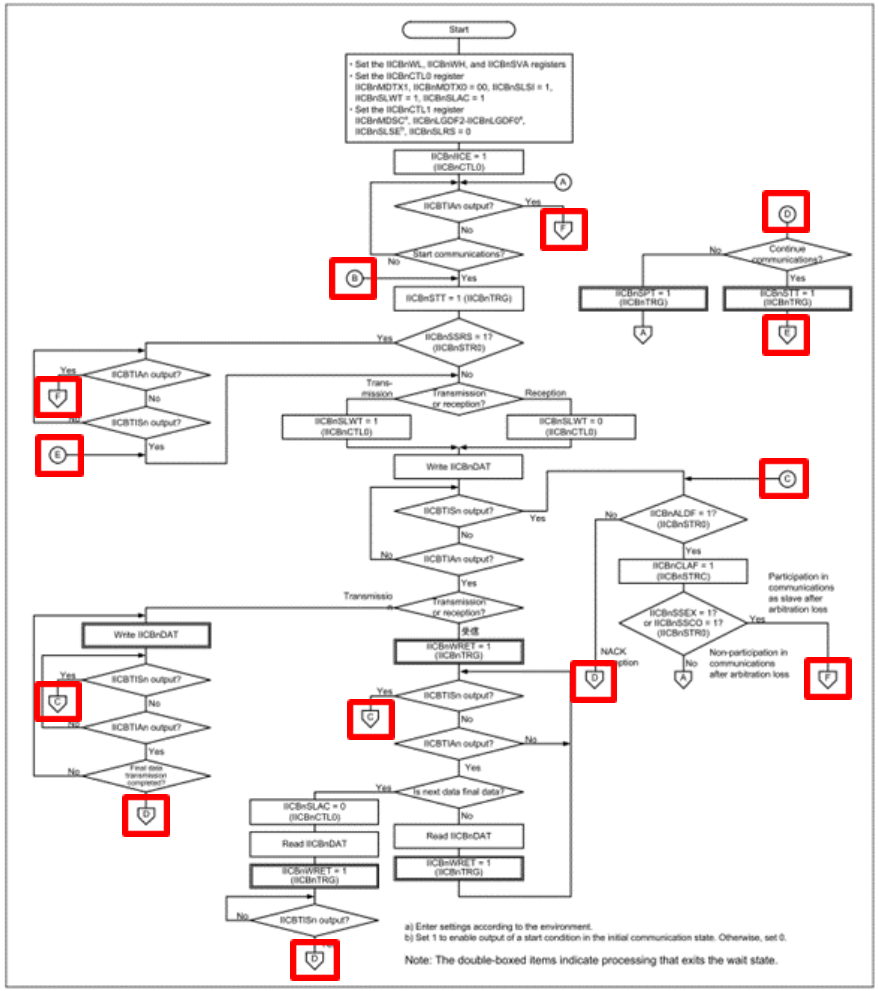
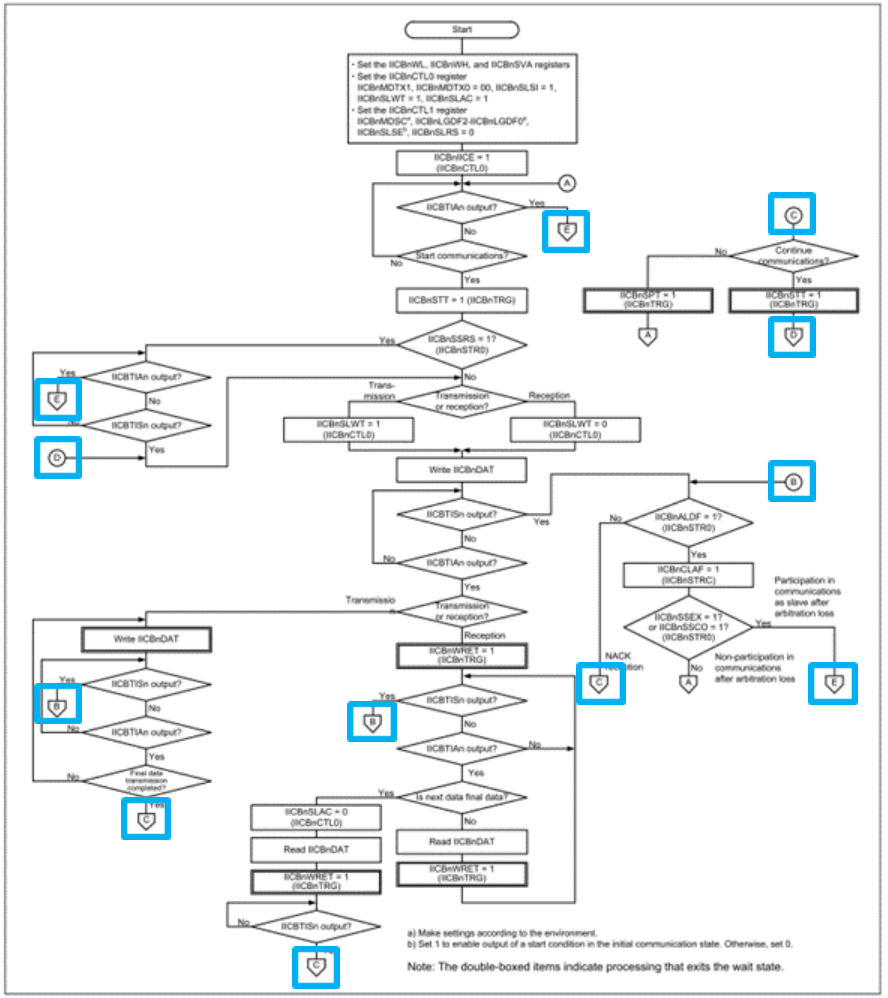
No. 226 18.9.1 (2) Slave operation setting procedure during single transfer mode

Titles of Section 18.9.1 (2) and Figure 18.15 modified. Branch description added.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>18-119</td><td>[18.9.1 (2) Slave operate setting sequence during single transfer mode]
[Figure 18.15 Slave operate setting sequence during single transfer mode (single master environment)]
 
</td><td>18-118</td><td>[18.9.1 (2) Slave operation setting procedure during single transfer mode]
[Figure 18.15 Slave Operation Setting Procedure during Single Transfer Mode (Single Master Environment)]
 
</td></tr>
</table>

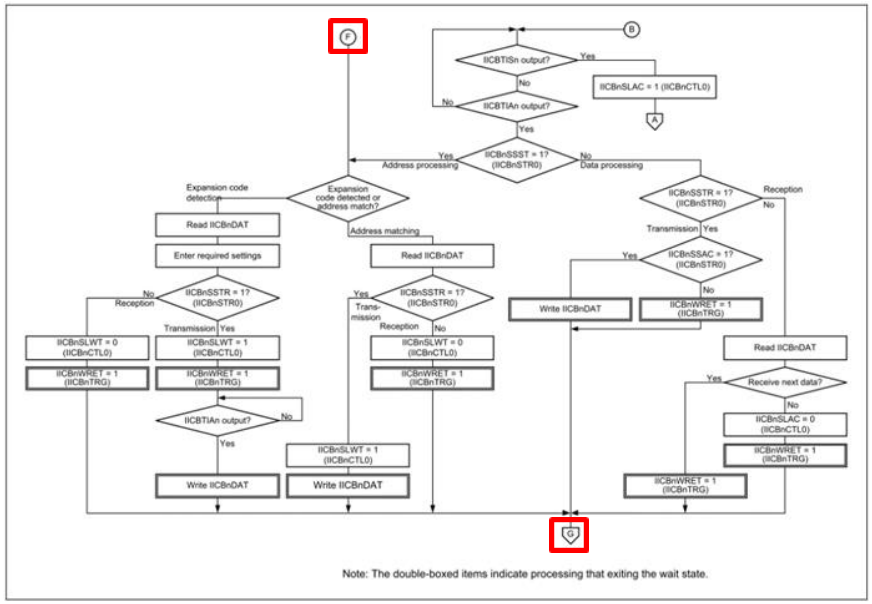
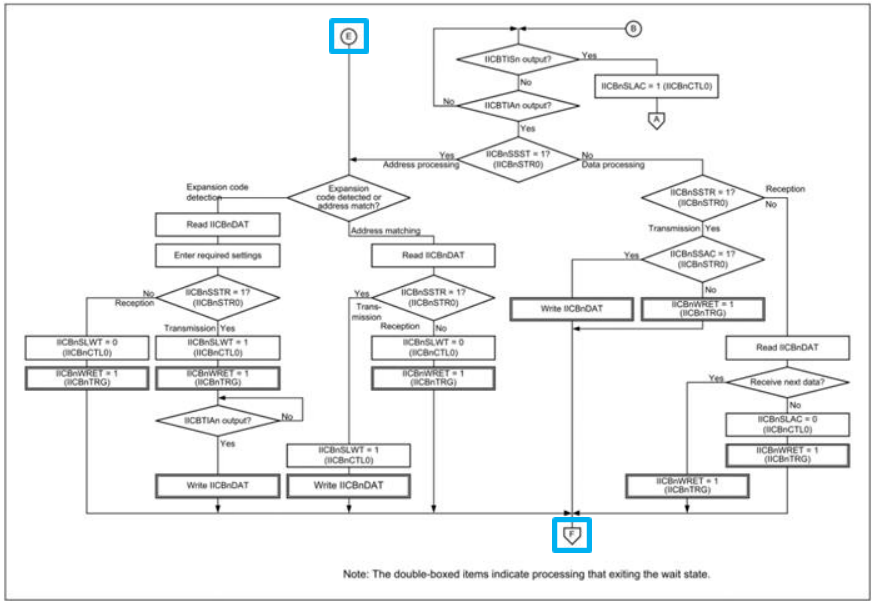
No. 227 18.9.2 (1) Single transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)

Titles of Section 18.9.2 (1) and Figure 18.18 modified. Labels of page connectors corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-122	**[18.9.2 (1) Single transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.18 Single transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0) (multi-master environment) (1/2)] 	18-121	**[18.9.2 (1) Single transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.18 Single Transfer Mode Setting Procedure when Communication Reserve Function is Enabled (IICBnCTL1.IICBnSLRS bit = 0) (Multi-Master Environment) (1/2)] 

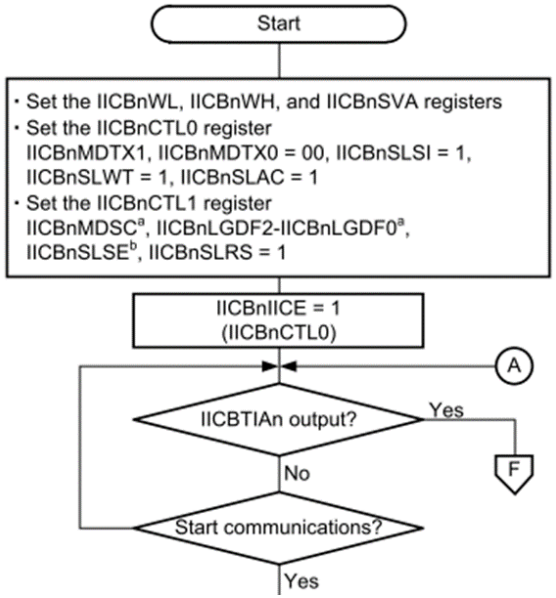
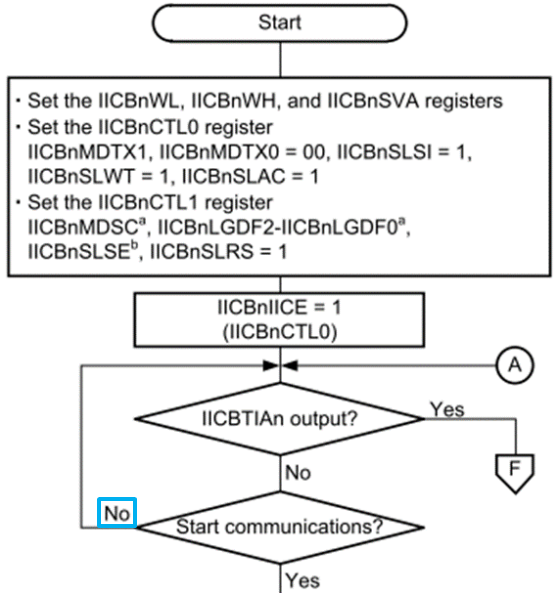
No. 228 18.9.2 (1) Single transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)

Labels of page connectors corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-123	**[18.9.2 (1) Single transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.18 Single transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0) (multi-master environment) (2/2)] 	18-122	**[18.9.2 (1) Single transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.18 Single Transfer Mode Setting Procedure when Communication Reserve Function is Enabled (IICBnCTL1.IICBnSLRS bit = 0) (Multi-Master Environment) (2/2)] 

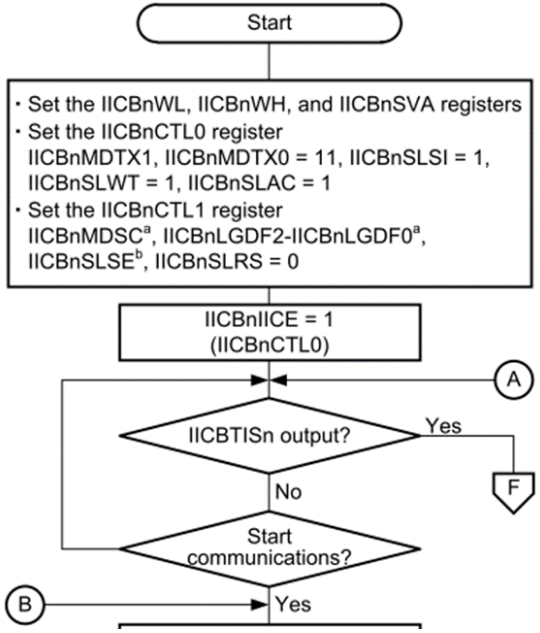
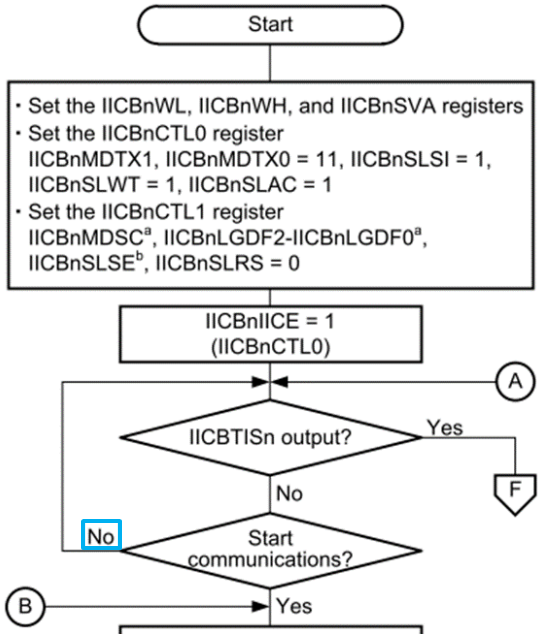
No. 229 18.9.2 (2) Single transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)

Titles of Section 18.9.2 (2) and Figure 18.19 modified. Branch label corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-124	**[18.9.2 (2) Single transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.19 Single transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1) (multi-master environment) (1/2)] 	18-123	**[18.9.2 (2) Single transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.19 Single Transfer Mode Setting Procedure when Communication Reserve Function is Disabled (IICBnCTL1.IICBnSLRS bit = 1) (Multi-Master Environment) (1/2)] 

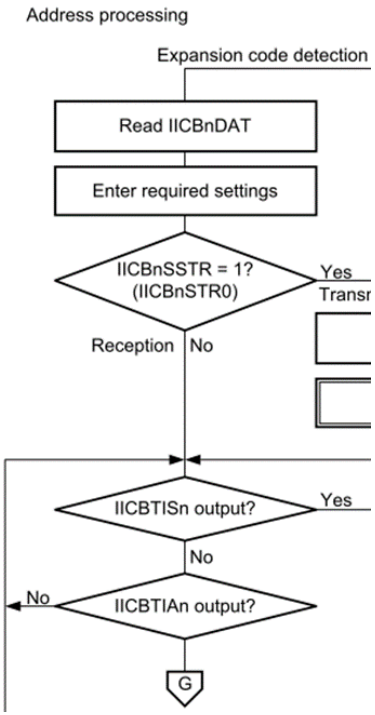
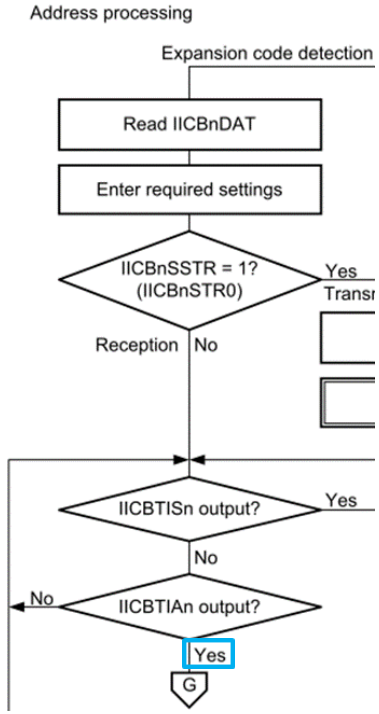
No. 230 18.9.2 (3) Continuous transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)

Titles of Section 18.9.2 (3) and Figure 18.20 modified. Branch label corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>18-126</td><td>[18.9.2 (3) Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]
[Figure 18.20 Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0) (multi-master environment) (1/2)]
 
</td><td>18-125</td><td>[18.9.2 (3) Continuous transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]
[Figure 18.20 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Enabled (IICBnCTL1.IICBnSLRS bit = 0) (Multi-Master Environment) (1/2)]
 
</td></tr>
</table>

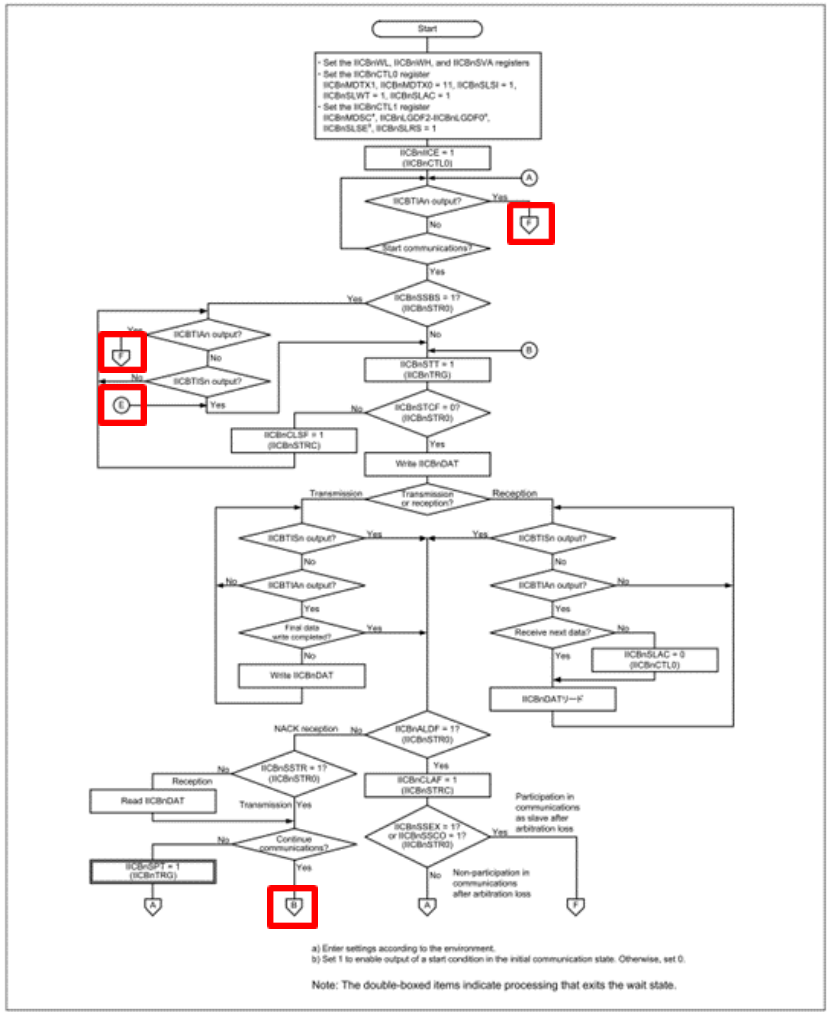
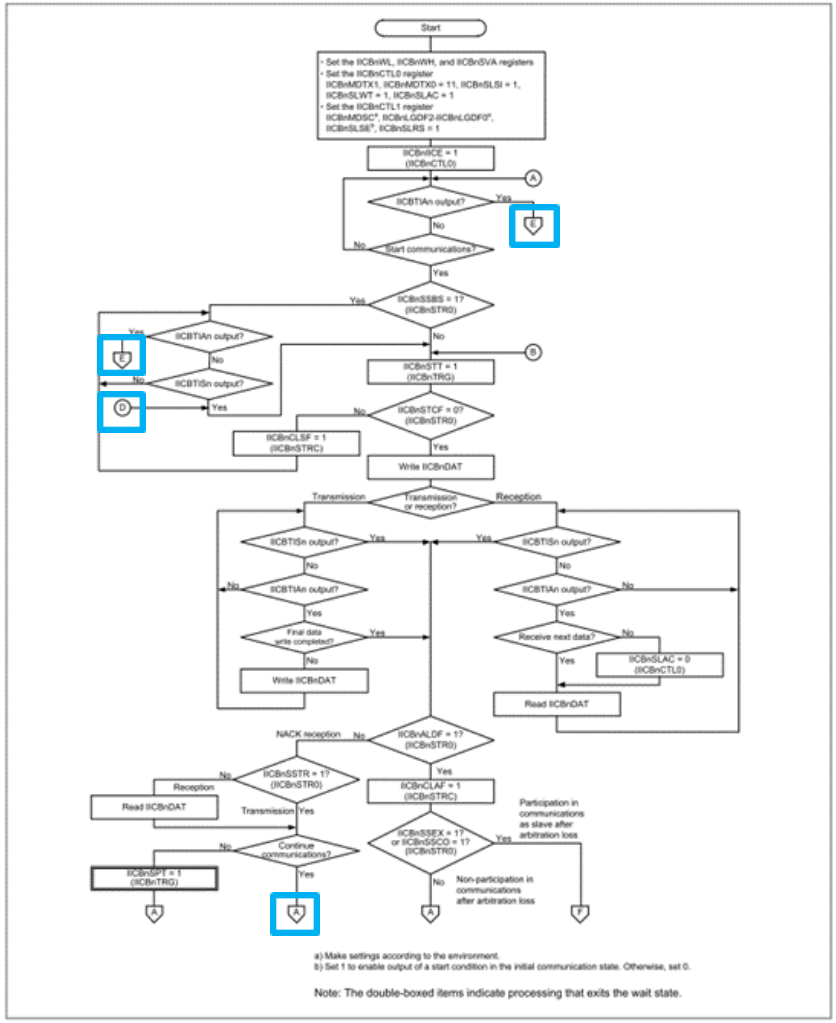
No. 231 18.9.2 (3) Continuous transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)

Branch label corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-127	**[18.9.2 (3) Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.20 Continuous transfer mode setting sequence when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0) (multi-master environment) (2/2)] 	18-126	**[18.9.2 (3) Continuous transfer mode setting procedure when communication reserve function is enabled (IICBnCTL1.IICBnSLRS bit = 0)]** [Figure 18.20 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Enabled (IICBnCTL1.IICBnSLRS bit = 0) (Multi-Master Environment) (2/2)] 

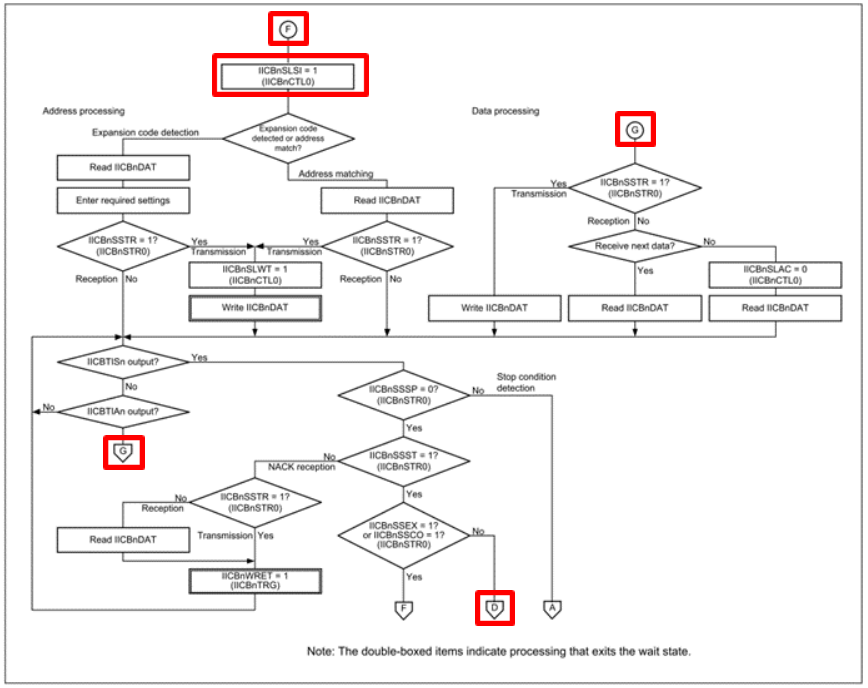
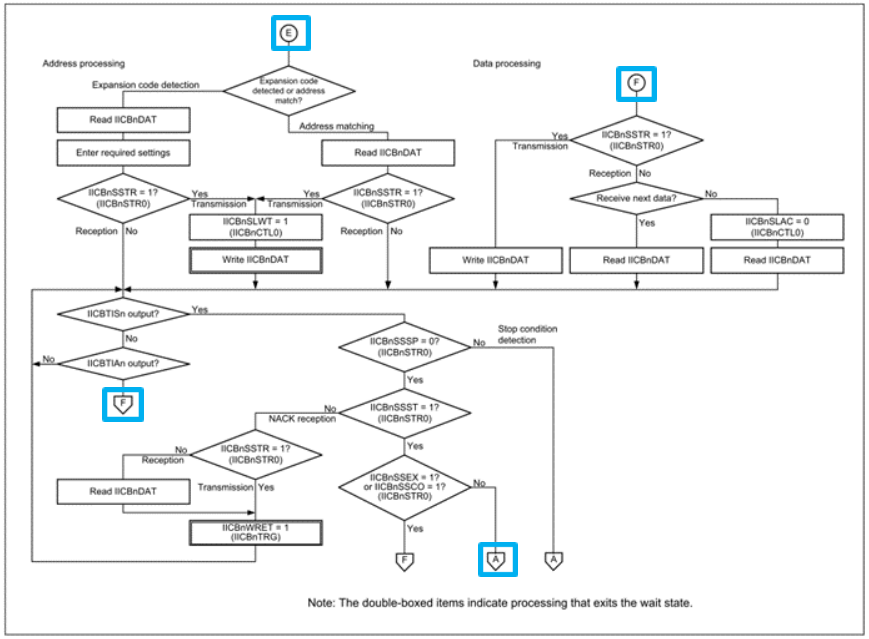
No. 232 18.9.2 (4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)

Titles of Section 18.9.2 (4) and Figure 18.21 modified. Labels of page connectors corrected.

V8.00		V9.00	
Page	Description	Page	Description
18-128	**[18.9.2 (4) Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.21 Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1) (multi-master environment) (1/2)]  	18-127	**[18.9.2 (4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]** [Figure 18.21 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Disabled (IICBnCTL1.IICBnSLRS bit = 1) (Multi-Master Environment) (1/2)] 

No. 233 18.9.2 (4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)

Process block in flow chart corrected. Labels of page connectors corrected.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>18-129</td><td>[18.9.2 (4) Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]
[Figure 18.21 Continuous transfer mode setting sequence when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1) (multi-master environment) (2/2)]
 
</td><td>18-128</td><td>[18.9.2 (4) Continuous transfer mode setting procedure when communication reserve function is disabled (IICBnCTL1.IICBnSLRS bit = 1)]
[Figure 18.21 Continuous Transfer Mode Setting Procedure when Communication Reserve Function is Disabled (IICBnCTL1.IICBnSLRS bit = 1) (Multi-Master Environment) (2/2)]
 
</td></tr>
</table>

No. 234 19. CAN Controller (FCN)

Introductory description of Section 19 modified.

V8.00		V9.00	
Page	Description	Page	Description
19-1	**[19. CAN Controller (FCN)]** The product features on-chip CAN (Controller Area Network) controllers that comply with the CAN protocol as standardized in ISO 11898. This chapter contains a generic description of the CAN Controller (FCN).	19-1	**[19. CAN Controller (FCN)]** This section explains the CAN (Controller Area Network) controllers that comply with the CAN protocol as standardized in ISO 11898.

No. 235 19. CAN Controller (FCN)

Introductory description of Section 19 modified.

V8.00		V9.00	
Page	Description	Page	Description
19-1	**[19. CAN Controller (FCN)]** The first section describes all R-IN32-M3 devices specific properties, such as instances, register base addresses, input/output signal names, etc. The subsequent sections describe the features that apply to all implementations.	19-1	**[19. CAN Controller (FCN)]** *(No entry)*

No. 236 19.1 Features of FCN

Title of Sub-Section 19.1 modified.

V8.00		V9.00	
Page	Description	Page	Description
19-1	**[19.1 FCN Features of R-IN32-M3]**	19-1	**[19.1 Features of FCN]**

No. 237 19.1 Features of FCN

Item “Clock supply” and [Table 19.3 CAN Controller Clock Supply] deleted.

V8.00		V9.00	
Page	Description	Page	Description
19-1	**[19.1 FCN Features of R-IN32-M3]** ○ Clock supply: All CAN Controllers provide one clock input. The CAN Controllers are connected to APB bus clock PCLK. Table 19.3 CAN Controller Clock Supply	19-1	**[19.1 Features of FCN]** *(No entry)* *(No entry)*

No. 238 19.1 Features of FCN

Title of item “Interrupts” and its description expanded. Title of Table 19.4 modified. Signal name corrected.

V8.00		V9.00	
Page	Description	Page	Description
19-2	**[19.1 FCN Features of R-IN32-M3]** ○ Interrupts: Table 19.4 shows the interrupts of the Can Controllers. [Table 19.4 FCNn interrupts and DMA requests] [INTC0REC, INTC0TRX, INTC0WUP INTC1REC, INTC1TRX, INTC1WUP] ・DMA controller trigger (DTFR/RTDFTR)	19-2	**[19.1 Features of FCN]** • Interrupts and peripheral modules: The following interrupt requests from FCN can be used as triggers for interrupt service routines or hardware ISRs (where listed as such), for DMA transfer (by the general-purpose DMAC or real-time port DMAC), for capture by a timer (TAUJ2), and for updating the real-time port pins (RP00-RP37). [Table 19.3 FCNn Interrupts and Requests for Peripheral Modules] [INTC0REC, INTC0TRX, INTC0WUP INTC1REC, INTC1TRX, INTC1WUP] • DMA controller trigger (DTFR/RTDTFR)

No. 239 19.3.2 (1) FCNn Global and Module Registers

Register name corrected.

V8.00		V9.00	
Page	Description	Page	Description
19-12	**[19.3.2 (1) FCNn global and module registers]** [Table 19.9 FCN1 global and module registers (2/2)] Register Name: FCN0*** register	19-12	**[19.3.2 (1) FCNn Global and Module Registers]** [Table 19.8 FCN1 Global and Module Registers (2/2)] Register Name: FCN1*** register

No. 240 19.5.2 (1) FCNn Module Mask Control Register (FCNnCMMKCTLaH, FCNnCMMKCTLaW)

Title of Section 19.5.2 (1) corrected.

V8.00		V9.00	
Page	Description	Page	Description
19-32	**[19.5.2 (1) FCNnCMMKCTLaH - FCNn module mask control register]**	19-31	**[19.5.2 (1) FCNn Module Mask Control Register (FCNnCMMKCTLaH, FCNnCMMKCTLaW)]**

No. 241 19.5.2 (3) FCNn Module Last Error Information Register (FCNnCMLCSTR)

Range of FCNnCMLCSSLC bits corrected.

V8.00		V9.00	
Page	Description	Page	Description
19-42	**[19.5.2 (3) FCNnCMLCSTR — FCNn module last error information register]** - Bit field: Bit[3:0] = FCNnCMLCSSLC[2:0] - Bit Position: 3 to 0	19-38	**[19.5.2 (3) FCNn Module Last Error Information Register (FCNnCMLCSTR)]** - Bit field: Bit[3:0] = 0, FCNnCMLCSSLC[2:0] - Bit Position: 2 to 0

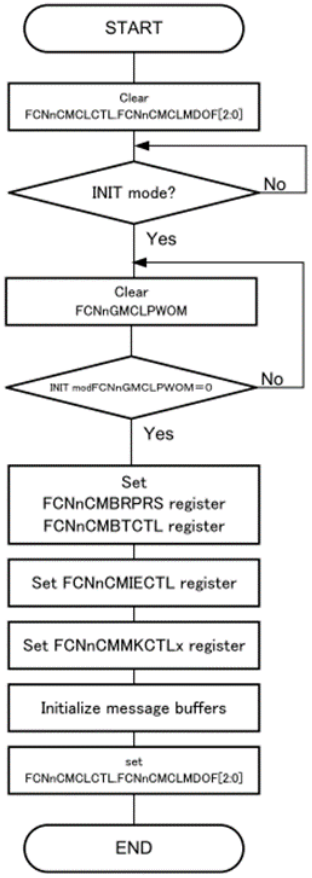
No. 242 19.13.1 Baud Rate Setting Conditions

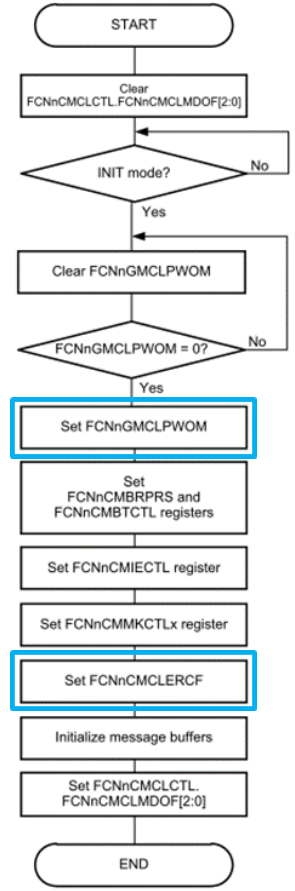
Expression of Baud rate setting conditions corrected.

V8.00		V9.00	
Page	Description	Page	Description
19-110	**[19.13.1 Baud rate setting conditions]** • 4 ≦ TSEG1[3:0] ≦ 16 [3 ≦ FCNnCMBTS1LG[3:0] ≦ 15]	19-99	**[19.13.1 Baud Rate Setting Conditions]** • 4 TQ ≤ TSEG1 ≤ 16 TQ [3 ≤ FCNnCMBTS1LG[3:0] ≤ 15]

No. 243 19.14.1 Initialization

Process blocks added to flow chart.

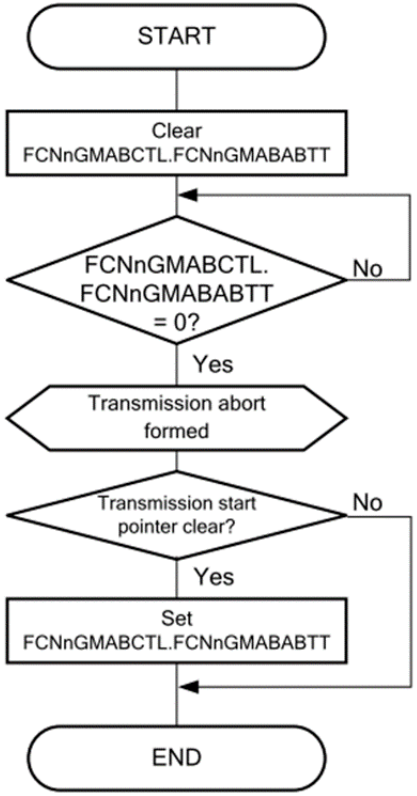
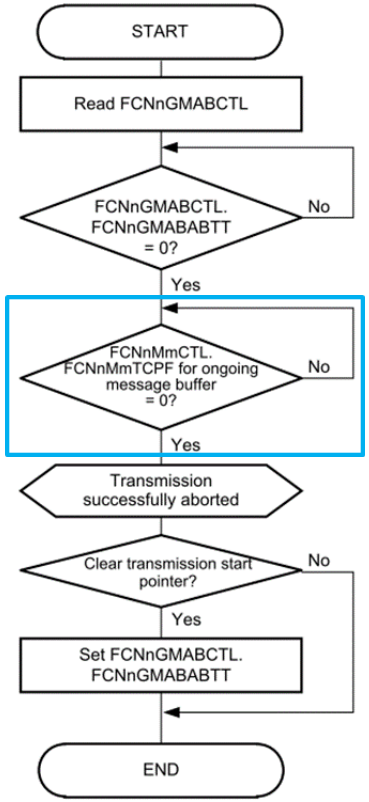
<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>19-117</td><td>[19.14.1 Initialization]
[Figure19.14 Re-initialization without using the software reset function]
 

Operation mode: Normal operation mode, normal operation mode with ABT, receive-only mode, single-shot mode, self-test mode</td><td>19-106</td><td>[19.14.1 Initialization]
[Figure 19.14 Re-initialization without Using the Software Reset]
 

Operation mode: Normal operation mode, normal operation mode with ABT, receive-only mode, single-shot mode, self-test mode</td></tr>
</table>

No. 244 19.14.2 Message Transmission

Decision block added to flow chart.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>19-133</td><td>[19.14.2 Message transmission]
[Figure19.28 ABT transmission request abort processing (normal operation mode with ABT) with transmission completely finished flag]
 
</td><td>19-122</td><td>[19.14.2 Message Transmission]
[Figure 19.28 ABT Transmission Request Abort Processing (in Normal Operation Mode with ABT) with Transmission Complete Flag]
 
</td></tr>
</table>

No. 245 20. CC-Link Interface

Supported stations updated.

V8.00		V9.00	
Page	Description	Page	Description
20-1	**[20. CC-Link Interface]** [Table 20.1 CC-Link Outline Specifications] Supported stations: Intelligent device station (TBD), Remote device station	20-1	**[20. CC-Link Interface]** [Table 20.1 CC-Link Outline Specifications] Supported stations Intelligent device station, Remote device station

No. 246 20.1.2 CC-Link Bus Size Control Register (CCBSC)

Description of CCBSC15-CCBSC0 bits added.

V8.00		V9.00	
Page	Description	Page	Description
20-2	**[20.1.2 CC-Link Bus Size Control Register (CCBSC)]** - Bit field: Bit[15:0] = 0 or 1 - R/W attribute: Bit[15:0] = 0 or 1 - Bit Position: 31 to 0 - Bit Name: – - Description: Set these bits to 0000 5575.	20-2	**[20.1.2 CC-Link Bus Size Control Register (CCBSC)]** - Bit field: Bit[15:0] = CCBSC15-CCBSC0 - R/W attribute: Bit[15:0] = R/W - Bit Position: 15 to 0 - Bit Name: CCBSC15-0 - Description: Set these bits to 5575H.

No. 247 20.1.2 CC-Link Bus Size Control Register (CCBSC)

Note 1 deleted.

V8.00		V9.00	
Page	Description	Page	Description
20-2	**[20.1.2 CC-Link Bus Size Control Register (CCBSC)]** Note 1. This register is only available in the R-IN32M3-CL. If you are using a device other than the R-IN32M3-CL, write 0 to these bits. When read, 0 is returned.	20-2	**[20.1.2 CC-Link Bus Size Control Register (CCBSC)]** *(No entry)*

No. 248 20.1.3 CC-Link Bus Bridge Control Register 0 (CCSMC0)

Description of CCSMC15-CCSMC0 bits added.

V8.00		V9.00	
Page	Description	Page	Description
20-2	**[20.1.3 CC-Link Bus Bridge Control Register 0 (CCSMC0)]** - Bit field: Bit[15:0] = 0 or 1 - R/W attribute: Bit[15:0] = 0 or 1 - Bit Position: 31 to 0 - Bit Name: – - Description: Set these bits to 0000 11b1H.	20-2	**[20.1.3 CC-Link Bus Bridge Control Register 0 (CCSMC0)]** - Bit field: Bit[15:0] = CCSMC15-CCSMC0 - R/W attribute: Bit[15:0] = R/W - Bit Position: 15 to 0 - Bit Name: CCSMC15-0 - Description: Set these bits to 11B1H.

No. 249 20.1.4 CC-Link Bus Bridge Control Register 1 (CCSMC1)

Description of CCSMC115-CCSMC10 bits added.

V8.00		V9.00	
Page	Description	Page	Description
20-3	**[20.1.4 CC-Link Bus Bridge Control Register 1 (CCSMC1)]** - Bit field: Bit[15:0] = 0 or 1 - R/W attribute: Bit[15:0] = 0 or 1 - Bit Position: 31 to 0 - Bit Name: – - Description: Set these bits to 0000 1131H.	20-3	**[20.1.4 CC-Link Bus Bridge Control Register 1 (CCSMC1)]** - Bit field: Bit[15:0] = CCSMC115-CCSMC10 - R/W attribute: Bit[15:0] = R/W - Bit Position: 15 to 0 - Bit Name: CCSMC115-0 - Description: Set these bits to 1131H.

No. 250 20.1.6 CC-Link Slave RUN LED Control Register (CCSRUN)

Figure 20.1 and its description added.

V8.00		V9.00	
Page	Description	Page	Description
20-4	**[20.1.6 CC-Link Slave RUN LED Control Register (CCSRUN)]** *(No entry)* *(No entry)*	20-4	**[20.1.6 CC-Link Slave RUN LED Control Register (CCSRUN)]** The figure below shows the circuit configuration of the CCSRUN register, CC-Link (intelligent device station and remote device station) RUN signals, and port pins. [Figure 20.1 Configuration of the CCSRUN Register and CC-Link (Intelligent Device Station and Remote Device Station) RUN Signals]

No. 251 21. System Registers (APB Peripheral Registers Area)

Title of Section 21 modified.

V8.00		V9.00	
Page	Description	Page	Description
21-1	**[21. Other Types of Interface Control]**	21-1	**[21. System Registers (APB Peripheral Registers Area)]**

No. 252 21.1 List of Registers

SRAM bridge select register (SRAMBRSEL) added.

V8.00		V9.00	
Page	Description	Page	Description
21-2	**[21.1 Registers]** *(No entry)*	21-2	**[21.1 List of Registers]** SRAM bridge select register SRAMBRSEL BASE+0804H YYYY

No. 253 21.3 IDCODE Register (IDCODE)

Description of IDCODE31-IDCODE0 bits added.

V8.00		V9.00	
Page	Description	Page	Description
21-3	**[21.3 IDCODE register]** - Bit field: 0 or 1 - R/W attribute: 0 or 1 - Bit Name: –	21-3	**[21.3 IDCODE Register (IDCODE)]** - Bit field: IDCODE31-IDCODE0 - R/W attribute: R - Bit Name: IDCODE31-0

No. 254 21.7 System Protect Command Register (SYSPCMD)

Caution 1 corrected.

V8.00		V9.00	
Page	Description	Page	Description
21-7	**[21.7 System protect command register (SYSPCMD)]** Caution 1. A value is not written to the register in steps <2> and <3>.	21-7	**[21.7 System Protect Command Register (SYSPCMD)]** Caution 1. A value is not written to the register in steps <1>, <2> and <3>.

No. 255 21.9.1 Timer Input Function Selection Register (SELCNT)

Names of TAUJ channels modified.

V8.00		V9.00	
Page	Description	Page	Description
21-10	**[21.9.1 Timer input function selection register (SELCNT)]** [Bit Position 7, 6: ISEL31, ISEL30] Specify the signal input to TIN3 (TAUJ23). Selection of TIN3 input signal (TAUJ23) [Bit Position 5, 4: ISEL21, ISEL20] Specify the signal input to TIN2 (TAUJ22). Selection of TIN2 input signal (TAUJ22)	21-10	**[21.9.1 Timer Input Function Selection Register (SELCNT)]** [Bit Position 7, 6: ISEL31, ISEL30] Specify the signal input to TIN3 (TAUJ2 ch3). Selection of TIN3 input signal (TAUJ ch3) [Bit Position 5, 4: ISEL21, ISEL20] Specify the signal input to TIN2 (TAUJ2 ch2). Selection of TIN2 input signal (TAUJ ch2)

No. 256 21.9.1 Timer Input Function Selection Register (SELCNT)

Names of TAUJ channels modified.

V8.00		V9.00	
Page	Description	Page	Description
21-11	**[21.9.1 Timer input function selection register (SELCNT)]** [Bit Position 3, 2: ISEL11, ISEL10] Specify the signal input to TIN1 (TAUJ21). Selection of TIN1 input signal (TAUJ21) [Bit Position 1, 0: ISEL01, ISEL00] Specify the signal input to TIN0 (TAUJ2). Selection of TIN0 input signal (TAUJ2)	21-11	**[21.9.1 Timer Input Function Selection Register (SELCNT)]** [Bit Position 3, 2: ISEL11, ISEL10] Specify the signal input to TIN1 (TAUJ2 ch1). Selection of TIN1 input signal (TAUJ ch1) [Bit Position 1, 0: ISEL01, ISEL00] Specify the signal input to TIN0 (TAUJ2 ch0). Selection of TIN0 input signal (TAUJ ch0)

No. 257 21.9.2 Timer Trigger Source Registers (TMTFR0 to TMTFR03)

Names of interrupts corrected.

V8.00		V9.00	
Page	Description	Page	Description
21-12	**[21.9.2 Timer trigger source registers (TMTFR0 to TMTFR03)]** - IFC6 to IFC0＝70H: CC-Link IE Field Network UDL WDTZ interrupt - IFC6 to IFC0＝78H:CC-Link slave RFSTB interrupt - IFC6 to IFC0＝79H: CC-Link slave MON3 interrupt	21-15	**[21.9.2 Timer Trigger Source Registers (TMTFR0 to TMTFR03)]** - IFC6 to IFC0＝70H: CC-Link IE Field WDTZ interrupt - IFC6 to IFC0＝78H: CC-Link REFSTB interrupt - IFC6 to IFC0＝79H: CC-Link MON3 interrupt

No. 258 21.10.1 Noise Filter Setting Registers 0 to 3 (NFC0 to NFC3)

Descriptions of bits 15-14, 13-12, 1-0 modified.

V8.00		V9.00	
Page	Description	Page	Description
21-17	**[21.10.1 Noise filter setting registers 0 to 3 (NFC0 to NFC3)]** [Bit Position 15, 14: NFPET11, NFPET10] Specify the number of cycles of the internal system clock at which the ETH1_GE_INT input is sampled to filter noise. [Bit Position 13, 12: NFPET01, NFPET00] Specify the number of cycles of the internal system clock at which the ETH0_GE_INT input is sampled to filter noise. [Bit Position 1, 0: NFPNM1, NFPNM0] Specify the number of cycles of the internal system clock at which the NMI input is sampled to filter noise.	21-17	**[21.10.1 Noise Filter Setting Registers 0 to 3 (NFC0 to NFC3)]** [Bit Position 15, 14: NFPET11, NFPET10] Specify the number of noise filter stages for the Ethernet 1 PHY interrupt signal (ETH1_GE_INT) input based on the number of cycles of the internal system clock. [Bit Position 13, 12: NFPET01, NFPET00] Specify the number of noise filter stages for the Ethernet 0 PHY interrupt signal (ETH0_GE_INT) input based on the number of cycles of the internal system clock. [Bit Position 1, 0: NFPNM1, NFPNM0] Specify the number of noise filter stages for the NMI input based on the number of cycles of the internal system clock.

No. 259 21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)

Section numbering scheme changed. Interrupt signals added.

V8.00		V9.00	
Page	Description	Page	Description
21-21	**[21.10.3 External interrupt mode registers 0, 1, 2 (INTM0, INTM1, INTM2)]** These registers are used to specify the trigger mode for the external interrupt requests input via external pins (NMIZ and INTPZ0 to INTPZ28).	21-21	**[21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)]** These registers are used to specify the trigger mode for the external interrupt requests input via external pins (NMIZ and INTPZ0 to INTPZ28, ETH1_GE_INT, ETH0_GE_INT).

No. 260 21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)

Names of interrupt signals modified.

V8.00		V9.00	
Page	Description	Page	Description
21-21	**[21.10.3 External interrupt mode registers 0, 1, 2 (INTM0, INTM1, INTM2)]** ○ INTM0: NMIZ, INTPHY1, INTPHY0	21-21	**[21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)]** ○ INTM0: NMIZ, ETH1_GE_INT, ETH0_GE_INT

No. 261 21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)

Names of interrupt signals modified. Notes deleted.

V8.00		V9.00	
Page	Description	Page	Description
21-22	**[21.10.3 External interrupt mode registers 0, 1, 2 (INTM0, INTM1, INTM2)]** [Bit Position 15, 14: ESE11, ESE10] Specify the trigger of INTPHY1 Trigger of INTPHY1 [Bit Position 13, 12: ESE01, ESE00] Specify the trigger of INTPHY0. Trigger of INTPHY0 Notes 1. If the active level (low) is input to the INTPZ0 to INTPZ28 pins, the input signal is judged as a successive pulse whose level toggles each time the internal system bus clock (HCLK) rises and an interrupt request is generated. HCLK, which is used to sample external interrupts, does not stop even in standby mode. 2. When the low level of NMIZ is detected, the inverted signal of the NMIZ pin is connected to the interrupt controller.	21-22	**[21.11 External Interrupt Mode Registers 0, 1, 2 (INTM0, INTM1, INTM2)]** [Bit Position 15, 14: ESE11, ESE10] Specify the trigger of Ethernet 1 PHY interrupt signal (ETH1_GE_INT). Trigger of ETH1_GE_INT [Bit Position 13, 12: ESE01, ESE00] Specify the trigger of Ethernet 0 PHY interrupt signal (ETH0_GE_INT). Trigger of ETH0_GE_INT *(No entry)*

No. 262 21.12.2 Trigger-Synchronous Port Source Registers (RP0TFR to RP3TFR)

Names of interrupts corrected.

V8.00		V9.00	
Page	Description	Page	Description
21-29	**[21.11.2 Trigger-synchronous port source registers (RP0TFR to RP3TFR)]** - IFC6 to IFC0＝70H: CC-Link IE Field Network UDL WDTZ interrupt - IFC6 to IFC0＝78H: CC-Link slave RFSTB interrupt - IFC6 to IFC0＝79H: CC-Link slave MON3 interrupt	21-29	**[21.12.2 Trigger-Synchronous Port Source Registers (RP0TFR to RP3TFR)]** - IFC6 to IFC0＝70H: CC-Link IE Field WDTZ interrupt - IFC6 to IFC0＝78H: CC-Link REFSTB interrupt - IFC6 to IFC0＝79H: CC-Link MON3 interrupt

No. 263 21.14 CPU Bus Operating Mode Register (CPUBUSMD)

Section numbering scheme changed.

V8.00		V9.00	
Page	Description	Page	Description
21-31	**[21.12 CPU Bus Operating Mode Register (CPUBUSMD)]**	21-31	**[21.14 CPU Bus Operating Mode Register (CPUBUSMD)]**

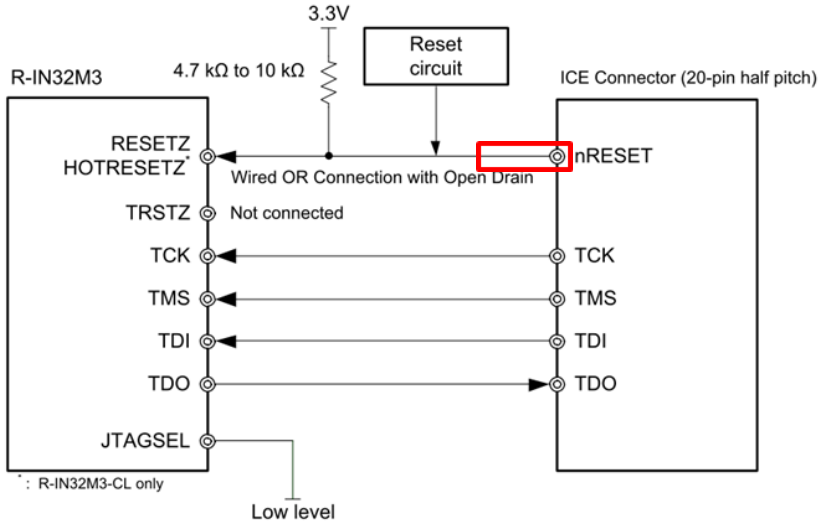
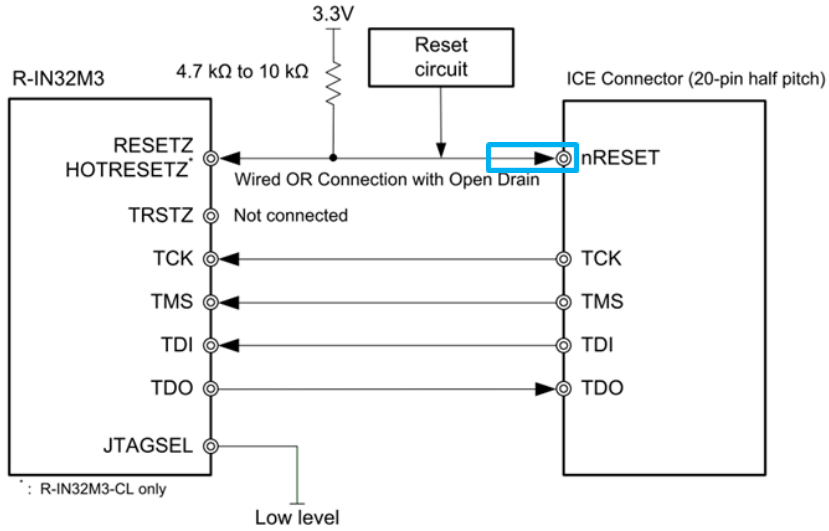
No. 264 21.15 SRAM Bridge Select Register (SRAMBRSEL)

Sub-Section [21.15 SRAM Bridge Select Register (SRAMBRSEL)] added.

V8.00		V9.00	
Page	Description	Page	Description
—	*(No entry)*	21-32	**[21.15 SRAM Bridge Select Register (SRAMBRSEL)]**

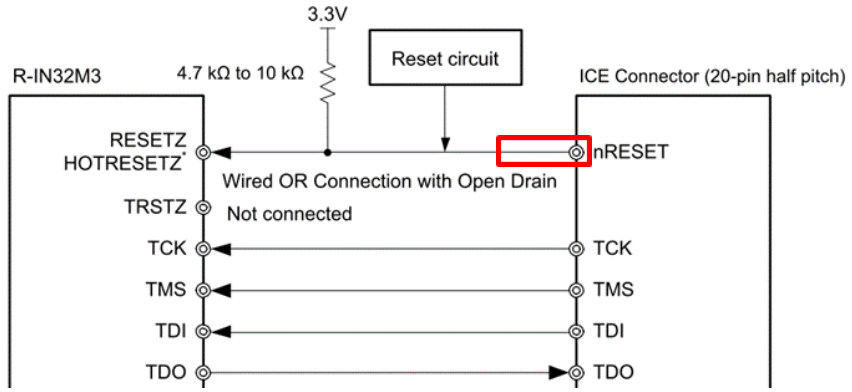
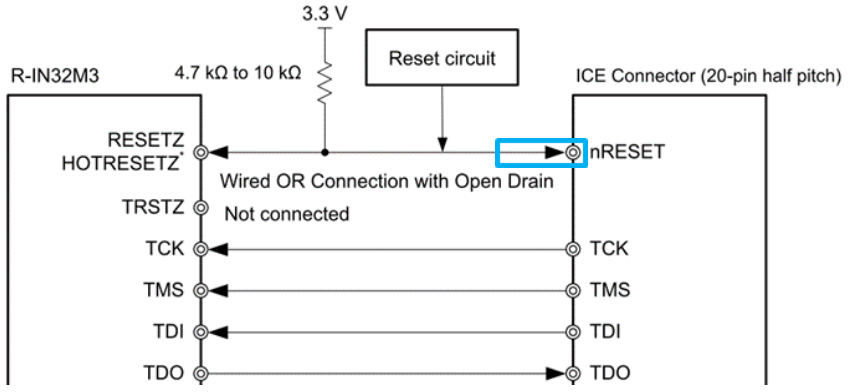
No. 265 22.1 JTAG interface

I/O arrow modified.

V8.00		V9.00	
Page	Description	Page	Description
22-1	**[22.1 JTAG interface]** [Figure 22.1 JTAG interface connection example (20-pin half pitch without trace)] 	22-1	**[22.1 JTAG interface]** [Figure 22.1 JTAG Interface Connection Example (20-Pin Half Pitch without Trace)] 

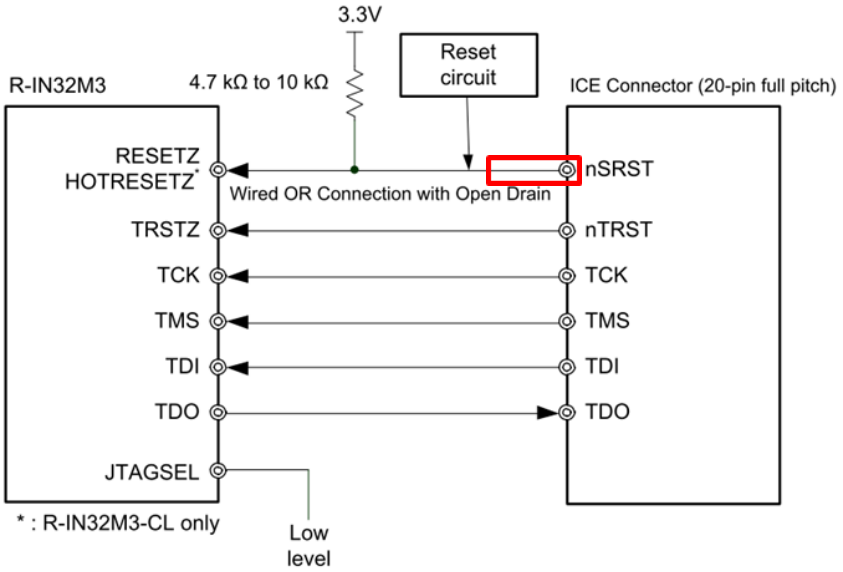
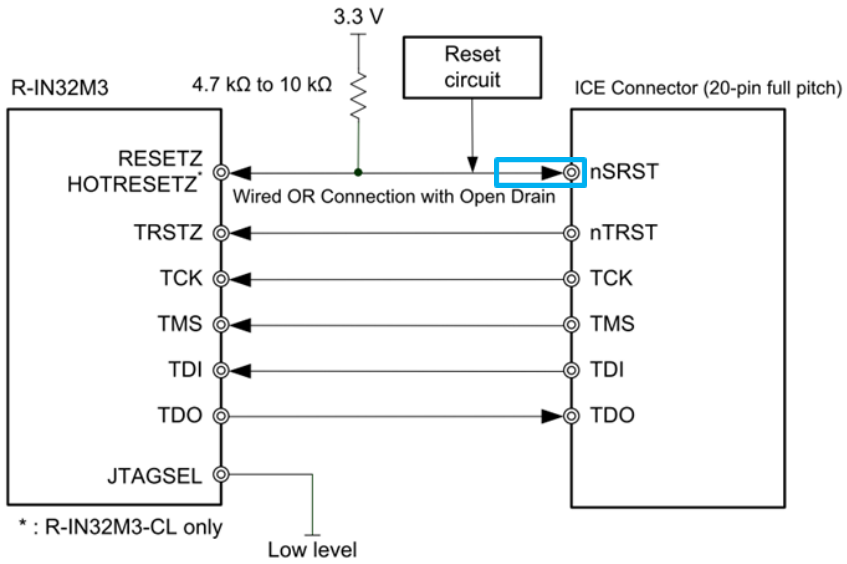
No. 266 22.1 JTAG interface

I/O arrow modified.

<table>
<tr><th colspan="2">V8.00</th><th colspan="2">V9.00</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>22-2</td><td>[22.1 JTAG interface]
[Figure 22.2 JTAG interface connection example (20-pin half pitch with trace)]
 
</td><td>22-2</td><td>[22.1 JTAG interface]
[Figure 22.2 JTAG Interface Connection Example (20-Pin Half Pitch with Trace)]
 
</td></tr>
</table>

No. 267 22.1 JTAG interface

I/O arrow modified.

V8.00		V9.00	
Page	Description	Page	Description
22-3	**[22.1 JTAG interface]** [Figure 22.3 JTAG interface connection example (20-pin full pitch)] 	22-3	**[22.1 JTAG interface]** [Figure 22.3 JTAG Interface Connection Example (20-Pin Full Pitch)] 

No. 268 22.1 JTAG interface

Note deleted.

V8.00		V9.00	
Page	Description	Page	Description
22-3	**[22.1 JTAG interface]** Note: Input “Low” to the JTAGSEL pin. When “High” is input, the system is set to boundary scan mode.	22-3	**[22.1 JTAG interface]** *(No entry)*