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RENESAS TECHNICAL UPDATE

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Product Category	System LSI	Document No.	TN-RIN-A008A/E	Rev.	1.00
Title	Notification of R-IN32M3 Series User's Manual Peripheral Modules (Rev.7.00 to Rev.8.00) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series User's Manual: Peripheral Modules R-IN32M3-EC, R-IN32M3-CL Rev8.00 (R18UZ0007EJ0800)	

R-IN32M3 Series User's Manual Peripheral Modules Rev. 8.00 (R18UZ0007EJ0800) has been released on Renesas website. For details, see "2. Documentation Updates" as below. In addition, as the item marked with "caution needed" may cause a failure on the device. Please confirm the item if it corresponds to your usage.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

(1/2)

No	Applicable Item (Rev.8.00 Section)	Applicable Page (Rev8.00)	Contents	
			MC-10287F1 UPD60510F1	MC-10287BF1 UPD60510BF1
1	1.1 Type Names of R-IN32M3-Series Products	p.1-1	Complement	←
	1.2 Base Addresses of the System Registers Area	p.1-1	Complement	←
2	2.2.2 Clock Control Registers (CLKGTD0, CLKGTD1)	p.2-5	Errors corrected	←
3	2.3.1 Overview	p.2-6	Complement	←
4	2.3.2 (1) Reset by signal input from a pin	p.2-6	Errors corrected	←
	2.3.2 (3) Reset by using software	p.2-6	Errors corrected	←
	2.3.2 (5) Reset output (RSTOUTZ output)	p.2-7	Complement	←
5	2.3.3 (1) System Reset Register (SYSRESET)	p.2-8	Errors corrected	←
6	2.3.4 Operations for Reset	p.2-9	Complement	←
7	4.1 Bus Occupancy by the Cortex-M3	p.4-2	-	Functions newly added
8	8.3.1(1) Management registers	p.8-3	-	Functions newly added
9	8.3.2.4 Ethernet Switch 10-Mbps Half-Duplex Mode Setting Register	p.8-9	-	Functions newly added
10	8.4.2.4 Hub Receive Filtering	p.8-73	Errors corrected	←
11	11. External MCU Interface	p.11-1	Complement	←
12	11.1 Memory MAP	p.11-3	Complement	←
13	11.2.2(3) Synchronous Mode and Asynchronous Mode	p.11-7	Errors corrected	←
14	11.2.3 Basic Motion Timing of External MCU Interface	p.11-9 to 11-11	Errors corrected	←
15	11.2.4(2) Timing adjustment (SRAM writing)	p.11-13	Errors corrected	←
16	11.2.4(3) Timing adjustment (SRAM read, page ROM read)	p.11-14	Errors corrected	←

(- : Excluded, ← : same as on the left)

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No	Applicable Item (Rev.8.00 Section)	Applicable Page (Rev8.00)	Contents	
			MC-10287F1 UPD60510F1	MC-10287BF1 UPD60510BF1
17	14.1 R-IN32M3 TAUJ2 Features	p.14-2	Complement	←
18	14.1.1 Timer operation functions	p.14-3	Functions newly added	←
19	14.3.3(3) TAUJ2CMORm - TAUJ2 channel mode OS register	p.14-15 to 14-18	Functions newly added	←
20	14.7.6 External Event Count Function	p.14-74 to 14-79	Functions newly added	←
21	15.3.2(2) WDTA Mode Register (WDTAnMD)	p.15-4	Errors corrected	←
22	17.1 Features of R-IN32M3 CSIH	p.17-2	Complement	←
23	18.9.1(3) Master operate setting sequence during continuous transfer mode *caution needed	p.18-120	Errors corrected	←
24	19.1 FCN Features of R-IN32-M3	p.19-2	Complement	←
25	19.13.2 Representative examples of baud rate settings *caution needed	p.19-114	Errors corrected	←
26	21.1 Registers	p.21-2	-	Functions newly added
27	21.4 Version register (RINVER)	p.21-4	-	Functions newly added
28	21.6 CPURESET register (CPURESET),	p.21-6	Complement	←
29	21.12 CPU Bus Operating Mode Register (CPUBUSMD)	p.21-31	-	Functions newly added

(- : Excluded, ← : same as on the left)

Incorrect and correct: highlighted in Yellow

1. 1. Introduction

“1.1 Type names of R-IN32M3-Series Products”, added.

“1. Introduction”, the second subsequent paragraphs moved and modified to “1.2 Base Addresses of the System Registers Area”. (p.1-1)

Rev7.00:

1. Introduction

This document has indicated the built-in peripheral function carried in industrial Ethernet-work LSI "R-IN32M3" series.
The register addresses shown below are relative addresses from the base address.
When accessing these registers via the external microcontroller interface, the base address is D_0000H. When accessing these registers from the CPU or DMA controller, the base address is 4001_0000H.

- When accessing from the CPU or DMA controller
  BASE = 4001_0000H
- When accessing via the external microcontroller interface
  BASE = D_0000H

Rev8.00:

1. Introduction

This document describes the internal peripheral modules of the R-IN32M3 series of industrial Ethernet network LSI chips.

1.1 Type Names of R-IN32M3-Series Products

In the type names of R-IN32M3-series (R-IN32M3-EC and R-IN32M3-CL) products, those of the current products include “B” while those of the old products do not.
Unless specially stated otherwise, the products mentioned in this manual are the current products.

Table 1.1 Type Names of R-IN32M3-Series Products

Product Name	Designation	Type Name	Features
R-IN32M3-EC	Current products	MC-10287BF1-HN4-A MC-10287BF1-HN4-M1-A	EtherCAT slave controller supported version
	Old products	MC-10287F1-HN4-A MC-10287F1-HN4-M1-A	
R-IN32M3-CL	Current products	UPD60510BF1-HN4-A UPD60510BF1-HN4-M1-A	CC-Link IE intelligent device station supported version
	Old products	UPD60510F1-HN4-A UPD60510F1-HN4-M1-A	

Caution: In the current products, the ETHSW10HDEN and CPUBUSMD registers have been newly added and the initial value of the RINVER register has been changed from that in the old products. For details, see the description of the following sections.
8.3.2.4, Ethernet Switch 10-Mbps Half-Duplex Mode Setting Register
21.4, Version register (RINVER)
21.12, CPU Bus Operating Mode Register (CPUBUSMD)

1.2 Base Addresses of the System Registers Area

This document has indicated the built-in peripheral function carried in industrial Ethernet-work LSI "R-IN32M3" series.
The register addresses shown below are relative addresses from the base address.
When accessing these registers via the external microcontroller interface, the base address is D_0000H. When accessing these registers from the CPU or DMA controller, the base address is 4001_0000H.

- When accessing from the CPU or DMA controller
  BASE = 4001_0000H
- When accessing via the external microcontroller interface
  BASE = D_0000H

2. 2.2.2 Clock Control Registers (CLKGTD0, CLKGTD1)

"Initial value" of CLKGTD1 register, modified. Note3 added. (p.2-5)

Rev7.00:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CLKGTD1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GCIE	GCCC	0	1	1	1	1	1	GCESW	GCCAT	GCWDT	GCFCN1	GCFCN0	GCCSI1	GCCSI0	BASE+ 01A4H Initial value 0000 6FFFH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	1	1	1	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 15	–	Reserved. When writing to these bits, write 0. When read, 0 is returned.
14	GCIE Note 1	CC-Link IE Field Network (slave) (1: Operating, 0: Stopped)
13	GCCC	CC-Link (1: Operating, 0: Stopped)
12	–	Reserved. When writing to this bit, write 0. When read, 0 is returned.
11 to 7	–	Reserved. When writing to these bits, write 1. When read, 1 is returned.
6	GCESW	Ethernet switch (1: Operating, 0: Stopped)
5	GCCAT Note 2	EtherCAT module (1: Operating, 0: Stopped)
4	GCWDT	Watchdog timer (1: Operating, 0: Stopped)
3	GCFCN1	CAN1 module (1: Operating, 0: Stopped)
2	GCFCN0	CAN0 module (1: Operating, 0: Stopped)
1	GCCSI1	CSI1 module (1: Operating, 0: Stopped)
0	GCCSI0	CSI0 module (1: Operating, 0: Stopped)

Notes1. This function is only available in the R-IN32M3-CL. When using a product other than the R-IN32M3-CL, write 0 to this bit. When read, 0 is returned.
2. This function is only available in the R-IN32M3-EC. When using a product other than the R-IN32M3-EC, write 0 to this bit. When read, 0 is returned.

Cautions1. Once the clock supply is stopped by using the CLKGTD register, it cannot be resumed. To supply the clock signal again, reset the system.
2. Access to stopped modules is prohibited. Operation is not guaranteed if an attempt is made to access these modules.

Rev8.00:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CLKGTD1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GCIE	GCCC	0	1	1	1	1	1	GCESW	GCCAT	GCWDT	GCFCN1	GCFCN0	GCCSI1	GCCSI0	BASE+ 01A4H Initial value Note 3
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	1	1	1	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 15	–	Reserved. When writing to these bits, write 0. When read, 0 is returned.
14	GCIE Note 1	CC-Link IE Field Network (slave) (1: Operating, 0: Stopped)
13	GCCC	CC-Link (1: Operating, 0: Stopped)
12	–	Reserved. When writing to this bit, write 0. When read, 0 is returned.
11 to 7	–	Reserved. When writing to these bits, write 1. When read, 1 is returned.
6	GCESW	Ethernet switch (1: Operating, 0: Stopped)
5	GCCAT Note 2	EtherCAT module (1: Operating, 0: Stopped)
4	GCWDT	Watchdog timer (1: Operating, 0: Stopped)
3	GCFCN1	CAN1 module (1: Operating, 0: Stopped)
2	GCFCN0	CAN0 module (1: Operating, 0: Stopped)
1	GCCSI1	CSI1 module (1: Operating, 0: Stopped)
0	GCCSI0	CSI0 module (1: Operating, 0: Stopped)

Notes1. This function is only available in the R-IN32M3-CL. When using a product other than the R-IN32M3-CL, write 0 to this bit. When read, 0 is returned.
2. This function is only available in the R-IN32M3-EC. When using a product other than the R-IN32M3-EC, write 0 to this bit. When read, 0 is returned.
3. The initial value depends on the product you are using.
R-IN32M3-CL: 0000 6FDFH
R-IN32M3-EC: 0000 2FFFH

Cautions1. Once the clock supply is stopped by using the CLKGTD register, it cannot be resumed. To supply the clock signal again, reset the system.
2. Access to stopped modules is prohibited. Operation is not guaranteed if an attempt is made to access these modules.

3. 2.3.1 Overview
Note added to HOTRESETZ. (p.2-6)

Rev7.00:

2.3.1 Overview
- Reset input via the RESETZ pin
- Power-on reset (including initialization of R-IN32M3 internal RAM) input via the PONRZ pin
- Reset input via the HOTRESETZ pin (available only in R-IN32M3-CL)
- Noise elimination for external reset pins based on analog delay (Applicable pins: RESETZ, PONRZ, HOTRESETZ Note, and TRSTZ)
- Reset control by using software
- Reset control by using watchdog timer (WDT)
- Reset output

Note: The HOTRESETZ pin is only available in the R-IN32M3-CL.

Rev8.00:

2.3.1 Overview
- Reset by signal input from the RESETZ pin
- Power-on reset by signal input from the PONRZ pin (including initialization of internal RAM of the R-IN32M3)
- Reset by signal input from the HOTRESETZ pin Note
- Noise elimination for external reset pins based on analog delay (Applicable pins: RESETZ, PONRZ, HOTRESETZ Note, and TRSTZ)
- Reset control by using software
- Reset control by using watchdog timer (WDT)
- Reset output

Note: The HOTRESETZ pin is only available in the R-IN32M3-CL.

* Applicable item except yellow hatched is unified description.

4. 2.3.2 Features

"(1) Reset input via a pin", part of description modified.
"(3) Reset by using software", RESETZ pin corrected to HOTRESETZ pin.
"Table 2.1 Reset Source and Targets to be Reset", Note2 added to CATRESET register. (p.2-6 to 2-7)

Rev7.00:

2.3.2 Features

(1) Reset input via a pin

When the reset signal PONRZ, RESETZ, or HOTRESETZ Note is input, the CPU core and on-chip peripheral functions are initialized. Note that inputting HOTRESETZ Note does not reset the internal PLL.

The low-level width of each reset signal must be at least 1 ms. However, in order for the external oscillator clock (25 MHz) to stabilize, the oscillation stabilization time must be included in the low level width of each reset pin. Also, at least two cycles of the external oscillator clock (25 MHz) must be supplied between when the low level of each reset pin is input and when the reset ends.

TRSTZ is only connected to the Cortex-M3 debugging unit. When resetting the CPU core and on-chip peripheral functions from the in-circuit emulator (ICE), connect the target reset signal (nTRST) input via the ICE connector to the RESETZ pin by using logic such as wired OR. In case of ICE half pitch connector, TRSTZ should be open. For details, see 22."Debugging".

Note: The HOTRESETZ pin is only available in the R-IN32M3-CL.

(2) Noise elimination for input reset signals

Noise at the external reset pins PONRZ, RESETZ, HOTRESETZ Note, and TRSTZ is eliminated based on analog delay. Signals shorter than 100 ns can be eliminated as noise.

Note: The HOTRESETZ pin is only available in the R-IN32M3-CL.

(3) Reset by using software

The R-IN32M3 can be reset by using the system reset register (SYSRESET). This reset is equivalent to a reset executed by inputting a signal to the RESETZ pin. With this method, the internal RAM is not reset.

(4) Reset by using the watchdog timer (WDT)

When a reset request is generated by the on-chip watchdog timer (WDT), the CPU core and on-chip peripheral functions are initialized. This reset is equivalent to a reset executed by inputting a signal to the RESETZ pin. With this method, the internal RAM is not reset.

(5) Reset output (RSTOUTZ output)

When a reset is generated in the R-IN32M3, a low-level signal is output from the RSTOUTZ pin. This reset can be used as a general reset for external devices.

Table 2.1 Reset Source and Targets to be Reset

Reset Source	Target to be Reset: Instruction RAM Data RAM Buffer RAM	PLL	CC-Link IE Field Network Note 1 Power on reset	CC-Link	EtherCAT Note 2	CPU's debugging unit	Other peripheral circuits
PONRZ pin	○	○	○	○	○	-	○
RESETZ pin	-	○	○	○	○	-	○
HOTRESETZ pin Note 1	-	-	-	○	○	-	○
TRSTZ pin	-	-	-	-	-	○	-
Watchdog timer	-	-	-	○	○	-	○
SYSRESET register	-	-	-	○	○	-	○
CPU reset	-	-	-	○	○	-	○
CCRES register	-	-	-	○	-	-	-
CATRESET register	-	-	-	-	○	-	-

Notes 1 Only the R-IN32M3-CL has.
2 Only the R-IN32M3-EC has.

Rev8.00:

2.3.2 Features

(1) Reset input via a pin

When the reset signal PONRZ, RESETZ, or HOTRESETZ Note is input, the CPU core and internal peripheral modules are initialized. Note that the input of HOTRESETZ Note does not reset the internal PLL.

The width at low level of each reset signal must be at least 1 µs. However, in order for oscillation to produce the external oscillator clock (25 MHz) to become stable, the oscillation stabilization time must be included in the width at low level for the signal on each reset pin.

TRSTZ is only connected to the Cortex-M3 debugging unit. When resetting the CPU core and internal peripheral modules from the in-circuit emulator (ICE), connect the target reset signal (nTRST) input via the ICE connector to the RESETZ pin by using logic such as wired OR. When using a half pitch connector as the ICE connector, it is recommended that TRSTZ should be open. For an example of the connection, see section 22 Debugging.

(2) Noise elimination for input reset signals

Noise at the external reset pins PONRZ, RESETZ, HOTRESETZ Note, and TRSTZ is eliminated based on analog delay. Signals shorter than 100 ns can be eliminated as noise.

(3) Reset by using software

The R-IN32M3 can be reset by using the system reset register (SYSRESET). This reset is equivalent to a reset executed by the input of a signal to the HOTRESETZ pin. The internal RAM is not initialized.

(4) Reset by using the watchdog timer (WDT)

When a reset request is generated by the on-chip watchdog timer (WDT), the CPU core and internal peripheral modules are initialized. This reset is equivalent to a reset executed by the input of a signal to the RESETZ pin. The internal RAM is not initialized.

Note: The HOTRESETZ pin is only available in the R-IN32M3-CL.

(5) Reset output (RSTOUTZ output)

When a reset is generated in the R-IN32M3, a low-level signal is output from the RSTOUTZ pin. This reset can be used as a general reset for external devices.

Table 2.1 Reset Source and Targets to be Reset

Reset Source	Target to be Reset: Instruction RAM Data RAM Buffer RAM	PLL	CC-Link IE Field Network Note 1 Power on reset	CC-Link	EtherCAT Note 2	CPU's debugging unit	Other peripheral circuits
PONRZ pin	✓	✓	✓	✓	✓	-	✓
RESETZ pin	-	✓	✓	✓	✓	-	✓
HOTRESETZ pin Note 1	-	-	-	✓	✓	-	✓
TRSTZ pin	-	-	-	-	-	✓	-
Watchdog timer	-	-	-	✓	✓	-	✓
SYSRESET register	-	-	-	✓	✓	-	✓
CPU reset	-	-	-	✓	✓	-	✓
CCRES register	-	-	-	✓	-	-	-
CATRESET register Note 2	-	-	-	-	✓	-	-

Notes 1 This is only provided in the R-IN32M3-CL.
2 This is only provided in the R-IN32M3-EC.

* Applicable item except yellow hatched is unified description.

5. 2.3.3(1) System reset register (SYSRESET)
HOTRESETZ input pin in the text corrected to HOTRESETZ input pin. (p.2-8)

Rev7.00:

(1) System reset register (SYSRESET)

R-IN32M3 is reset (an equivalent for a RESETZ input terminal). The register of the object of a PONRZ terminal is not reset. Reset release of this register is performed when carrying out reset release of R-IN32M3.

Rev8.00:

(1) System Reset Register (SYSRESET)

This register resets the R-IN32M3 (equivalent to the HOTRESETZ input pin). The register for the PONRZ pin is not reset. This register is used to release the R-IN32M3 from the reset state.

* Applicable item except yellow hatched is unified description.

6. 2.3.4 Operations for Reset

“Figure 2.2 Timing of Reset at Power On”, RSTOUTZ waveform added. (p.2-9)

Rev7.00:

2.3.4 Reset behavior

Below charts shows reset behavior at power on and system reset of R-IN32M3 series.

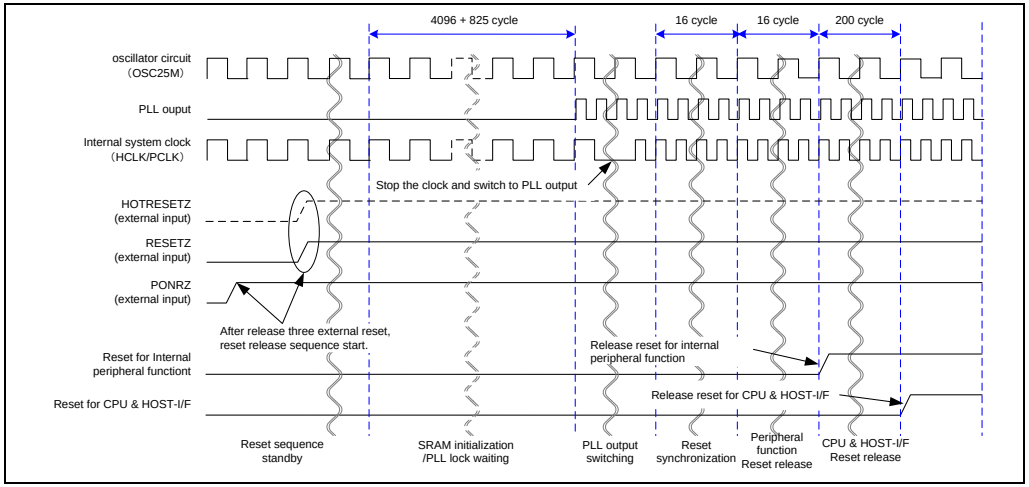


Figure 2.2 Timing of Reset at Power On

Rev8.00:

2.3.4 Operations for Reset

The charts below show the timing of the reset at power on and when a system reset is issued for the R-IN32M3 series.

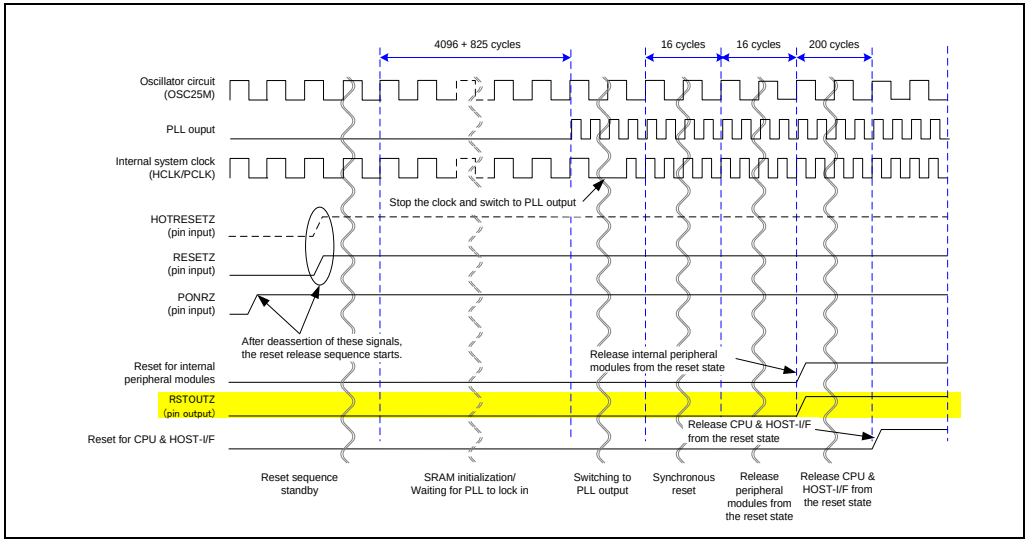


Figure 2.2 Timing of Reset at Power On

* Applicable item except yellow hatched is unified description.

7. 4.1 Bus Occupancy by the Cortex-M3

"4.1 Bus Occupancy by the Cortex-M3", added. (p.4-2)

Rev7.00:

No descriptions.

Rev8.00:

4.1 Bus Occupancy by the Cortex-M3

By default, when the Cortex-M3 of an R-IN32M3-series device successively copies data within a given memory, it proceeds with burst transfer of the required length and occupies the bus over that period, making other masters wait for access to the memory. The period over which another master must wait for access thus depends on the period of continuous access by the Cortex-M3.

To reduce the period over which other masters are kept waiting for access, set the CPU bus operation mode register (CPUBUSMD) to change the form of transfer by the Cortex-M3 to single transfer. This allows access by other masters even during continuous access by the Cortex-M3.

8. 8.3.1(1) Management registers

"(1) Management registers", ETHSW10HDEN register added. (p.8-3)

Rev7.00:

(1) Management registers

Register name	Symbol	Address
Ethernet PHY LINK mode resister	ETHPHYLNK	BASE + 0614H
Ethernet switch management TAG control register	ETHSWMTC	BASE + 0680H
Ethernet switch operating mode setting register	ETHSWMD	BASE + 0684H

Rev8.00:

(1) Management registers

Register name	Symbol	Address
Ethernet PHY LINK mode resister	ETHPHYLNK	BASE + 0614H
Ethernet switch management TAG control register	ETHSWMTC	BASE + 0680H
Ethernet switch operating mode setting register	ETHSWMD	BASE + 0684H
Ethernet switch 10-Mbps half-duplex mode setting register	ETHSW10HDEN	BASE + 060C

9. 8.3.2.4 Ethernet Switch 10-Mbps Half-Duplex Mode Setting Register

“8.3.2.4 Ethernet Switch 10-Mbps Half-Duplex Mode Setting Register”, added. (p.8-9)

Rev7.00:

No descriptions.

Rev8.00:

8.3.2.4 Ethernet Switch 10-Mbps Half-Duplex Mode Setting Register

This register is for disabling the looping back of received frames by the Ethernet PHY layer during transmission when the Ethernet switch is used for 10-Mbps half-duplex communications.

The Ethernet PHY layer of the R-IN32M3-EC loops back transmitted data to received data in 10-Mbps half-duplex transfer. If Ethernet switching by this LSI chip is used to set up a loopback between two ports, transfer is mutually repeated between these ports, and Ethernet transfer does not proceed successfully.

- Access This register can be read and written in 32- or 16-bit units.

Cautions 1. This register is only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register.
2. Only select disabling of received frames while the Ethernet PHY layer is linked in half-duplex communications at 10 Mbps. If this is done in another linked state, some correct received frames may also be disabled.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
ETHSW 10HDEN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW10HDEN1	SW10HDEN0	BASE +060CH 初期値 0000 0000H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	

Bit Position	Bit Name	Description
31 to 2	–	Reserved. When writing to these bits, write 0. If read, 0 is returned.
1	SW10HDEN1	Disables looping back of received frames during transmission from Ethernet port 1. 0: Disabling is not selected (this should be set when operation is other than for 10-Mbps half-duplex communications). 1: Disabling is selected (this should only be set when operation is for 10-Mbps half-duplex communications).
0	SW10HDEN0	Disables looping back of received frames during transmission from Ethernet port 0. 0: Disabling is not selected (this should be set when operation is other than for 10-Mbps half-duplex communications). 1: Disabling is selected (this should only be set when operation is for 10-Mbps half-duplex communications).

Notes 1. This register is only supported by the R-IN32M3-EC.
2. The old products do not support this register.
For details of the old products, see section 1.1, Type Names of R-IN32M3-Series Products <R>.

10. 8.4.2.4 Hub Receive Filtering

"Table 8.7 Typical HUB MAC Filter Setup", entries under "Notes", corrected. (p.8-73)

Rev7.00:

Table 8.7 Typical HUB MAC Filter Setup

MAC Address	Mask	Force Forward	Notes
01-80-c2-00-00-00	0xC0	0	Filters all frames in range 01-80-c2-00-00-{00..3F} The register settings for MAClo/hi would be: HUB_FLT_MACnlo= 0x00C28001 HUB_FLT_MACnhi= 0x00C00000
01-1b-19-00-00-00	0xFF	0	Filters only this address (PTPv2)
01-00-5e-00-01-80	0xF8	0	Filters 01-00-5e-00-01-{80..87}(224.0.1.{128..135})
01-00-5e-00-00-00	0xFC	0	Filters 01-00-5e-00-00-{00..03} (224.0.0.{0..3})
<local node unicast address>	0xFF	0	Should be entered to avoid unnecessary forwarding of frames that are directed to the node only.
01-21-6C-00-00-01	0xFF	1	Should be force forwarded through the HUB. The register settings for MAClo/hi would be: HUB_FLT_MACnlo= 0x006C2101 HUB_FLT_MACnhi= 0x01FF0100

Rev8.00:

Table 8.7 Typical HUB MAC Filter Setup

MAC Address	Mask	Force Forward	Notes
01-80-c2-00-00-00	0xC0	0	Filters all frames in range 01-80-c2-00-00-{00..3F} The register settings for MAClo/hi would be: HUB_FLT_MACnlo= 0x00C28001 HUB_FLT_MACnhi= 0x00C00000
01-1b-19-00-00-00	0xFF	0	Filters only this address (PTPv2)
01-00-5e-00-01-80	0xF8	0	Filters 01-00-5e-00-01-{80..87}(224.0.1.{128..135})
01-00-5e-00-00-00	0xFC	0	Filters 01-00-5e-00-00-{00..03} (224.0.0.{0..3})
<local node unicast address>	0xFF	0	Should be entered to avoid unnecessary forwarding of frames that are directed to the node only.
01-21-6C-00-00-01	0xFF	1	Should be force forwarded through the HUB. The register settings for MAClo/hi would be: HUB_FLT_MAC6lo= 0x006C2101 HUB_FLT_MAC6hi= 0x01FF0100

11. 11. External MCU Interface

"Table 11.1 Mode of the External MCU Interface Selected by the Level on the Operating Mode Setting Pin", added (p.11-1)

Rev7.00:

11. External MCU Interface

In order to use the internal resource of the external host MPU to an R-IN32M3, the external MCU interface is established.

The external MCU interface is interface to connect external MPU. External MCU I/F's signal is assigned same ports to both use with Asynchronous SRAM MEMC and synchronous burst access MEMC, and can be used as external MCU interface in case of setting MEMIFSEL to High level. Please set MEMIFSEL pin level until to release reset from the later one of PONRZ or RESETZ after power supply. The dynamic switching isn't supported.

When using an external MCU interface, the boot of an R-IN32M3 can use external MCU boot or serial flash ROM boot. However, an external memory accessing function (external ROM/SRAM) cannot be used.

The external MCU interface is equivalent to the asynchronous SRAM interface and the synchronous SRAM interface. When the level of a HIFSYNC pin is high-level, it becomes a synchronous SRAM interface, and when HIFSYNC is a low level, it becomes an asynchronous SRAM interface.

Moreover, the external MCU interface supports the synchronous SRAM type transmission of a clock synchronizer type so that mass data can be accessed at high speed. MEMIFSEL pin and MEMCSEL pin can be used by making it high-level.

Rev8.00:

11. External MCU Interface

In order to use the internal resource of the external host MPU to an R-IN32M3, the external MCU interface is established.

The external MCU interface is interface to connect external MPU. External MCU I/F's signal is assigned same ports to both use with Asynchronous SRAM MEMC and synchronous burst access MEMC, and can be used as external MCU interface in case of setting MEMIFSEL to High level. Please set MEMIFSEL pin level until to release reset from the later one of PONRZ or RESETZ after power supply. The dynamic switching isn't supported.

When using an external MCU interface, the boot of an R-IN32M3 can use external MCU boot or serial flash ROM boot. However, an external memory accessing function (external ROM/SRAM) cannot be used.

The external MCU interface is equivalent to the asynchronous SRAM interface and the synchronous SRAM interface. When the level of a HIFSYNC pin is high-level, it becomes a synchronous SRAM interface, and when HIFSYNC is a low level, it becomes an asynchronous SRAM interface.

Moreover, the external MCU interface supports the synchronous SRAM type transmission of a clock synchronizer type so that mass data can be accessed at high speed. MEMIFSEL pin and MEMCSEL pin can be used by making it high-level.

Table 11.1 Mode of the External MCU Interface Selected by the Level on the Operating Mode Setting Pin

MEMIFSEL	MEMCSEL	HIFSYNC	ADMUXMODE	Function
Low	—	—	—	Not accessible from the external MCU (operating mode of the external memory interface)
High	Low	Low	Low	Asynchronous SRAM interface mode is entered. Connection of the bus clock signal to HBUSCLK is not required.
			High	Setting prohibited
		High	Low	Synchronous SRAM interface mode is entered. Connection of the bus clock signal to HBUSCLK is required.Note
			High	Setting prohibited
	High	Low	Low	Setting prohibited
			High	Setting prohibited
		High	Low	Setting prohibited
			High	Synchronous SRAM type transfer mode is entered.

Note: For access to the CC-Link IE field, synchronous SRAM interface mode must be set (MEMIFSEL = high, MEMCSEL = low, HIFSYNC = high). The CC-Link IE field is only included in the R-IN32M3-CL.

12. 11.1 Memory MAP
“Figure 11.1 External MCU interface Space”, Note3 added. (p.11-3)

Rev7.00:

11.1 Memory MAP

2M byte area is prepared as an external microcomputer interface.

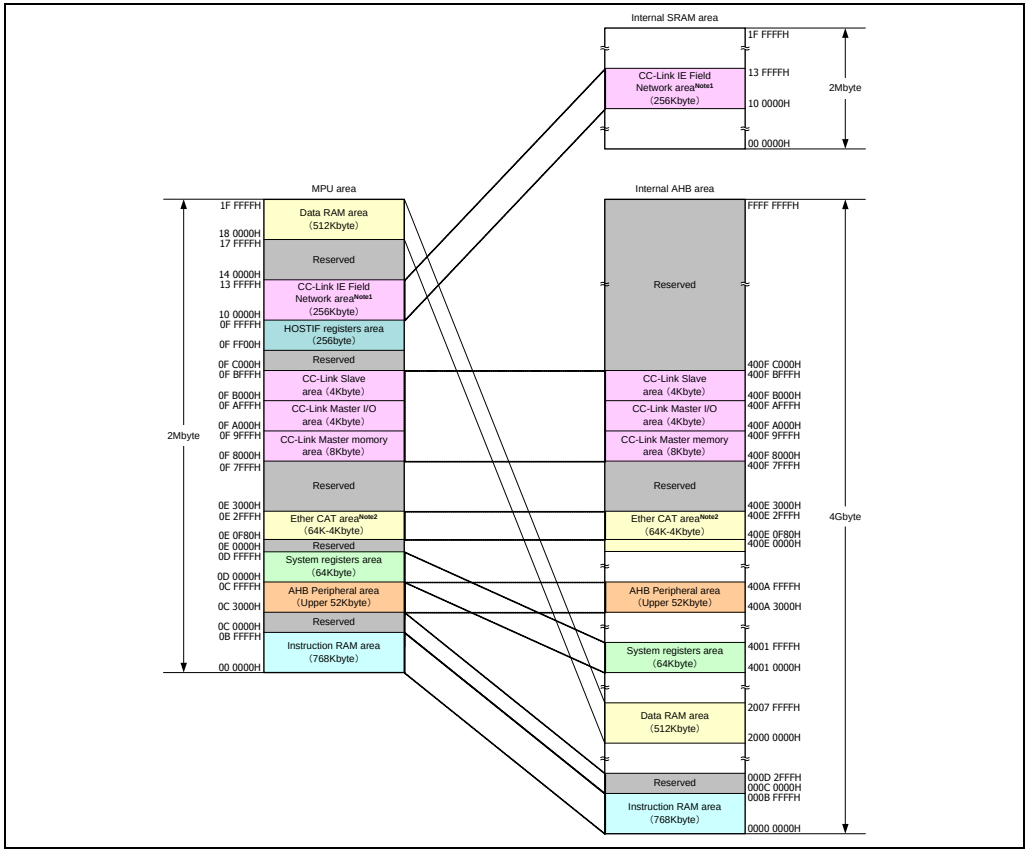


Figure 11.1 External MCU interface Space

Notes 1. Only the R-IN32M3-CL version has.
2. Only the R-IN32M3-EC version has.

Rev8.00:

11.1 Memory MAP

A 2 Mbyte space is provided as the external MCU interface.

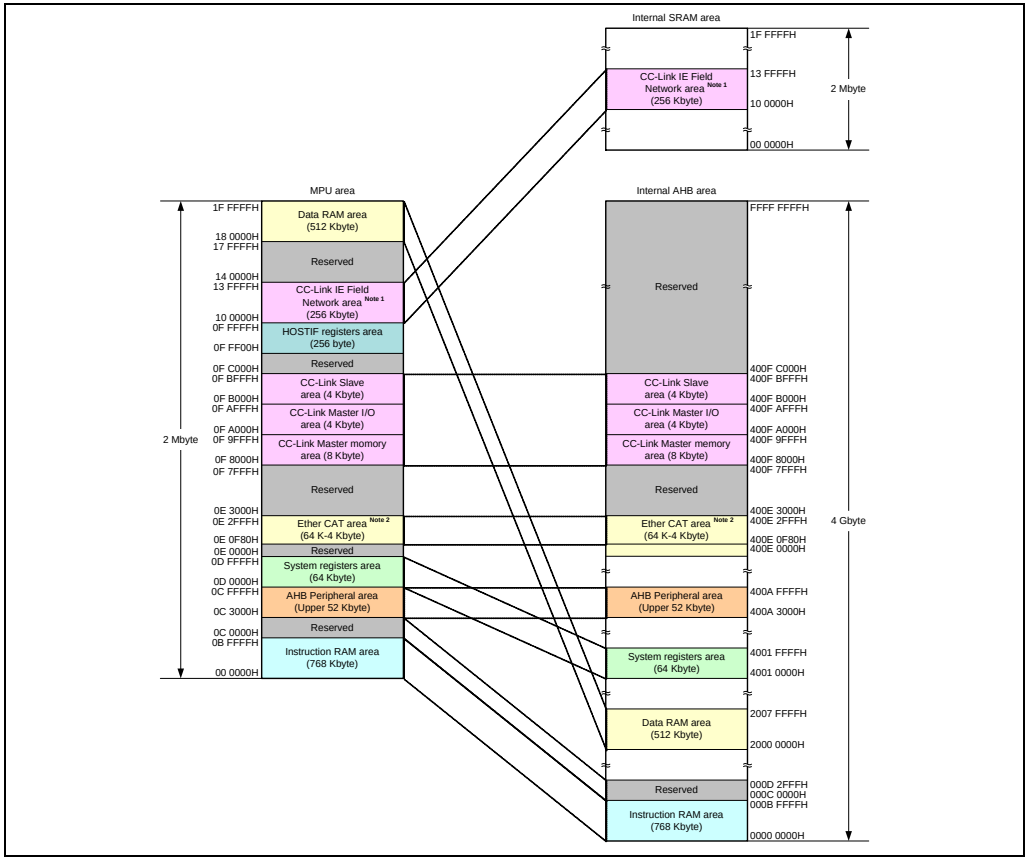


Figure 11.1 External MCU interface Space

Notes 1. This is only provided in the R-IN32M3-CL.
2. This is only provided in the R-IN32M3-EC.
3. The upper 52 Kbytes of the AHB peripheral registers area covers the range from the GPIO area to the synchronous burst memory controller control registers. For details, see the memory map of the R-IN32M3 Series User’s Manual.

* Applicable item except yellow hatched is unified description.

13. 11.2.2(3) Synchronous Mode and Asynchronous Mode

"Table11.4 Synchronous relation of an external MCU interface", changed. (p.11-7)

Rev7.00:

Table11.4 Synchronous relation of an external MCU interface

Signal Name	I/O	HIFSYNC (Synchronous Relation Selection)	
		H (Synchronous Mode)	L (Asynchronous Mode)
HCSZ	Input	HBUSCLK synchronous	Asynchronous
HPGCSZ	Input	HBUSCLK synchronous	Asynchronous
HA20-HA1	Input	HBUSCLK synchronous	Asynchronous
HRDZ	Input	HBUSCLK synchronous	Asynchronous
HWRSTBZ	Input	HBUSCLK synchronous	Asynchronous
HWRZ3-HWRZ0, HBENZ3-HBENZ0	Input	HBUSCLK synchronous	Asynchronous
HD31-HD0 (input)	Input	HBUSCLK synchronous	Asynchronous
HD31-HD0 (output)	Output	Asynchronous	Asynchronous
HWAITZ	Output	HBUSCLK synchronous	Asynchronous
HERROUTZ	Output	Asynchronous	

Rev8.00:

Table11.4 Synchronous relation of an external MCU interface

Signal Name	I/O	HIFSYNC (Synchronous Relation Selection)		
		H (Synchronous Mode)		L (Asynchronous Mode)
		Write	Read	
HCSZ	Input	HBUSCLK synchronous	Asynchronous	Asynchronous
HPGCSZ	Input	HBUSCLK synchronous	Asynchronous	Asynchronous
HA20-HA1	Input	HBUSCLK synchronous	Asynchronous	Asynchronous
HRDZ	Input	—	Asynchronous	Asynchronous
HWRSTBZ	Input	HBUSCLK synchronous	—	Asynchronous
HWRZ3-HWRZ0, HBENZ3-HBENZ0	Input	HBUSCLK synchronous	—	Asynchronous
HD31-HD0 (input)	Input	HBUSCLK synchronous	—	Asynchronous
HD31-HD0 (output)	Output	—	Asynchronous	Asynchronous
HWAITZ	Output	HBUSCLK synchronous		Asynchronous
HERROUTZ	Output	Asynchronous		

14. 11.2.3 Basic Motion Timing of External Microcomputer Interface

"Figure 11.2 Write to CC-Link IE Field Network Area (SRAM write)" to "Figure 11.5 Read from External MCU Interface Register Area (SRAM read)", changed. "11.2.3 (3) Access to Other Area", added. (p.11-9 to 11-11)

Rev7.00:

11.2.3 Basic Motion Timing of External Microcomputer Interface
(1) Access to a CC-Link IE Field Network area

Remark: Only in the R-IN32M3-CL has this function.

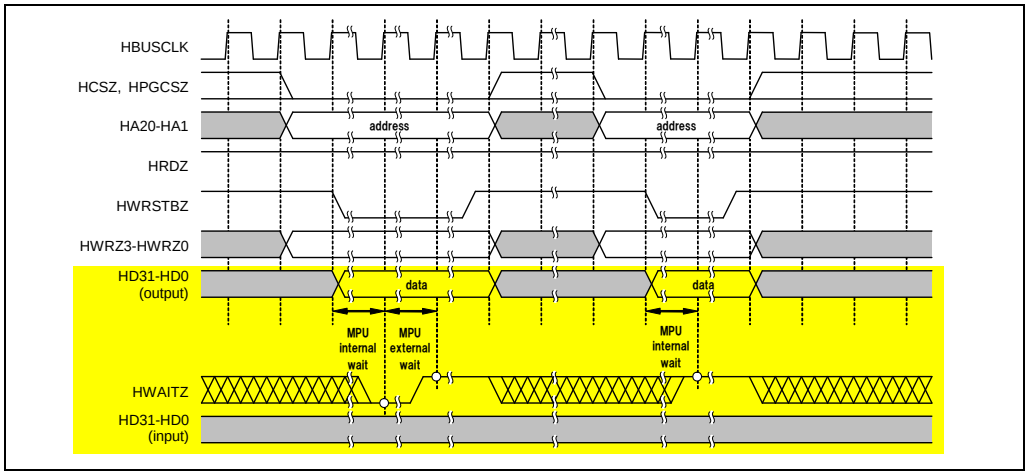


Figure 11.2 Write to a CC-Link IE Field Network area (SRAM write)

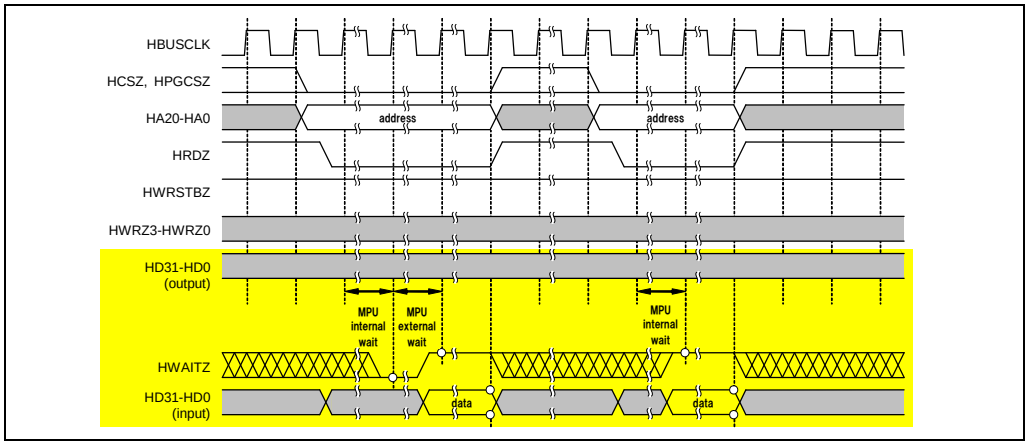


Figure 11.3 Read from CC-Link IE Field Network area (SRAM read)

Rev8.00:

11.2.3 Basic Motion Timing of External Microcomputer Interface
(1) Access to CC-Link IE Field Network Area

Remark: Only in the R-IN32M3-CL has this function.

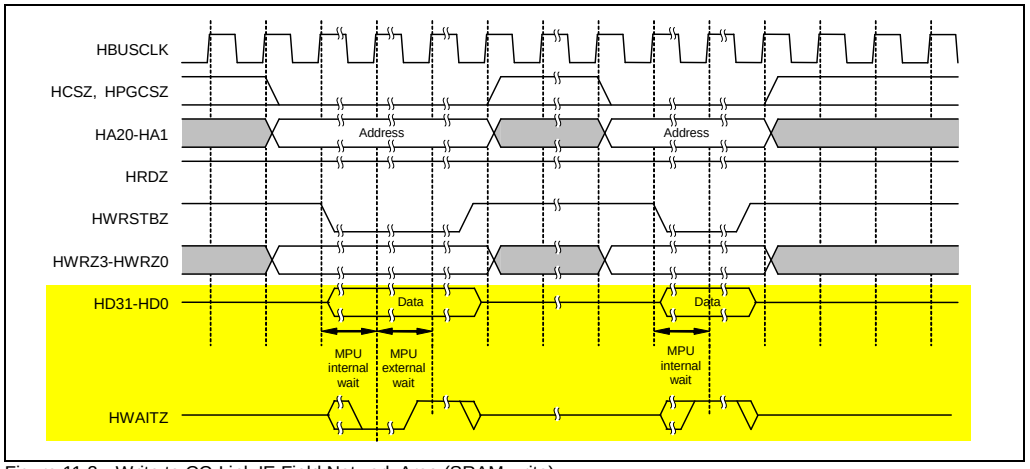


Figure 11.2 Write to CC-Link IE Field Network Area (SRAM write)

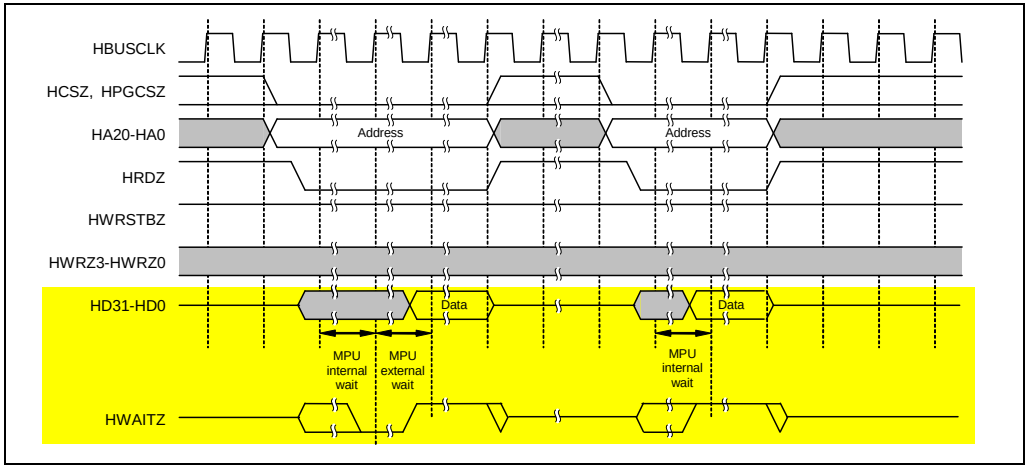


Figure 11.3 Read from CC-Link IE Field Network Area (SRAM read)

14. 11.2.3 Basic Motion Timing of External Microcomputer Interface

"Figure 11.2 Write to CC-Link IE Field Network Area (SRAM write)" to "Figure 11.5 Read from External MCU Interface Register Area (SRAM read)", changed. "11.2.3 (3) Access to Other Area", added. (p.11-9 to 11-11) continued

Rev7.00:

(2) Access to a external MPU interface register area

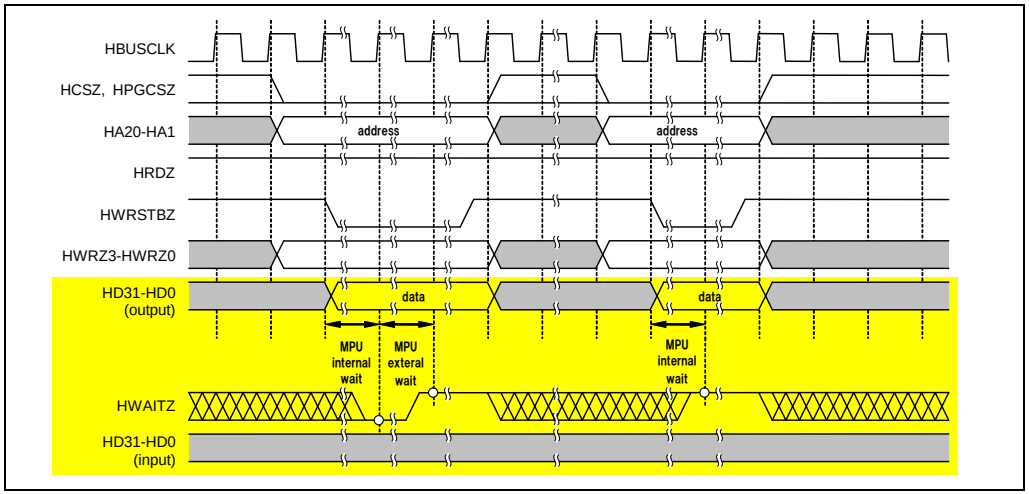


Figure11.4 Write to a external MPU interface register area (SRAM write)

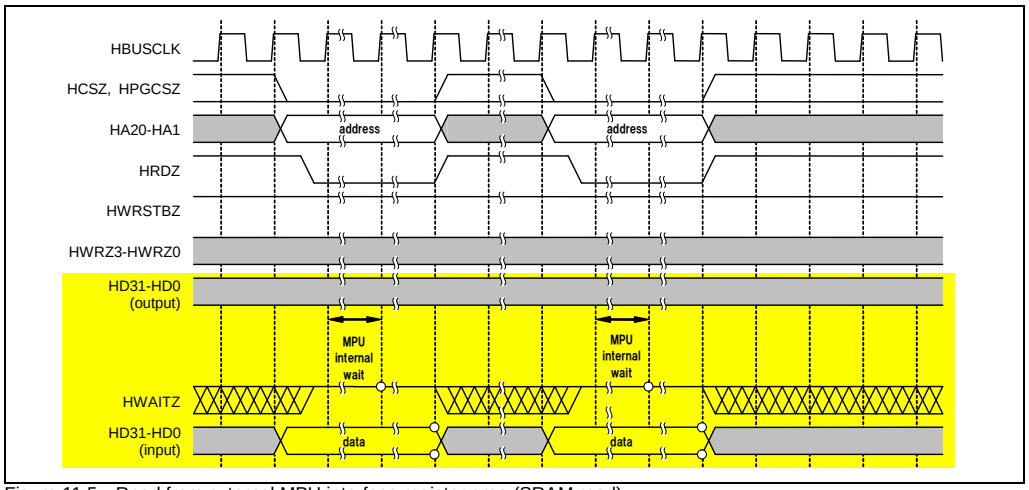


Figure 11.5 Read from external MPU interface register area (SRAM read)

Rev8.00:

(2) Access to External MCU Interface Register Area

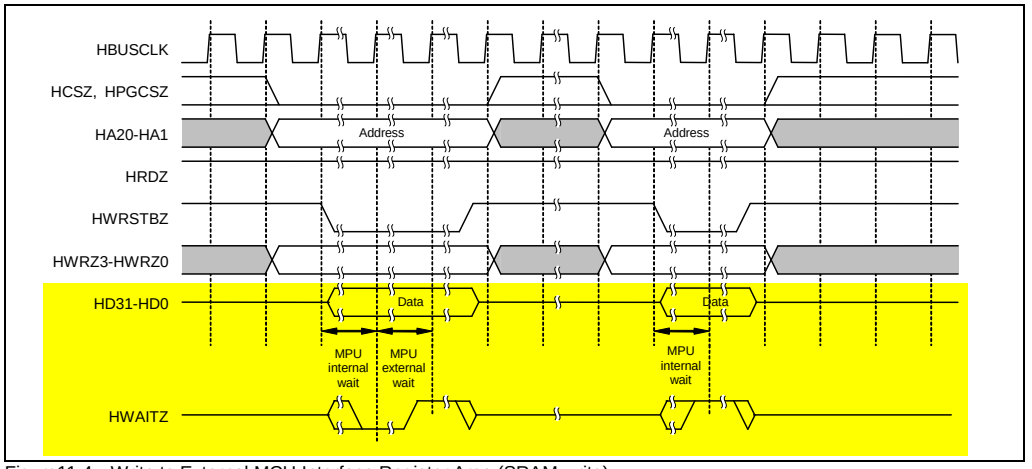


Figure11.4 Write to External MCU Interface Register Area (SRAM write)

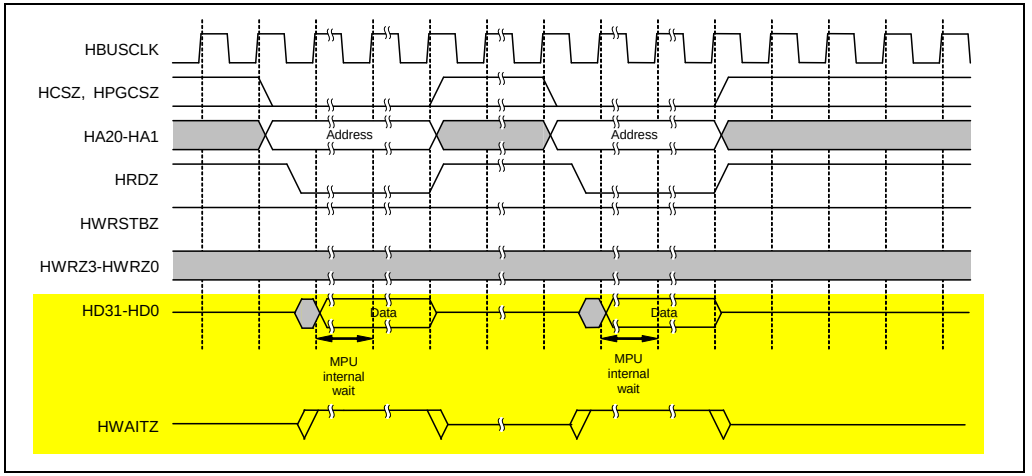


Figure 11.5 Read from External MCU Interface Register Area (SRAM read)

14. 11.2.3 Basic Motion Timing of External Microcomputer Interface
"Figure 11.2 Write to CC-Link IE Field Network Area (SRAM write)" to "Figure 11.5 Read from External MCU Interface Register Area (SRAM read)", changed.
"11.2.3 (3) Access to Other Area", added. (p.11-9 to 11-11) continued

Rev7.00:

No descriptions.

Rev8.00:

(3) Access to Other Area

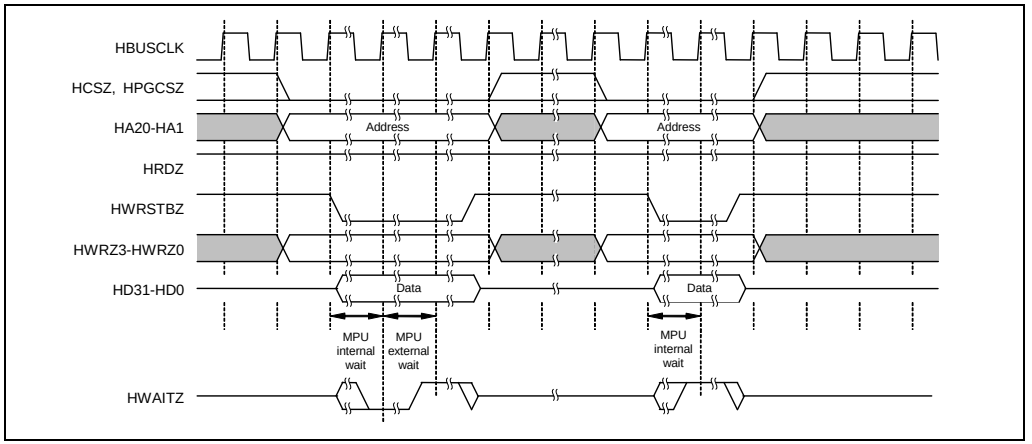


Figure 11.6 Write to Other Area (SRAM write)

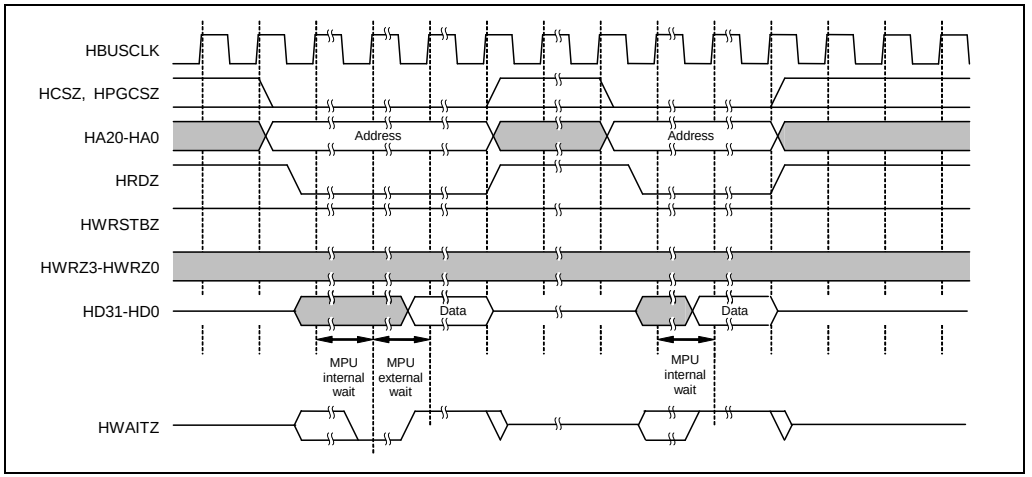


Figure 11.7 Read from Other Area (SRAM read)

15. 11.2.4(2) Timing adjustment (SRAM writing)

"Figure 11.8 Timing Adjustment (SRAM writing)", changed. (p.11-13)

Rev7.00:

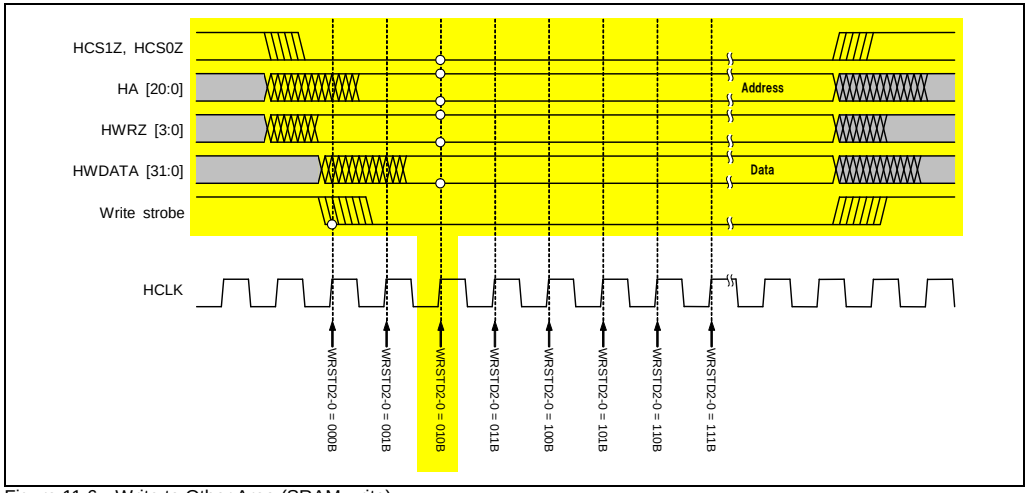


Figure 11.6 Write to Other Area (SRAM write)

Rev8.00:

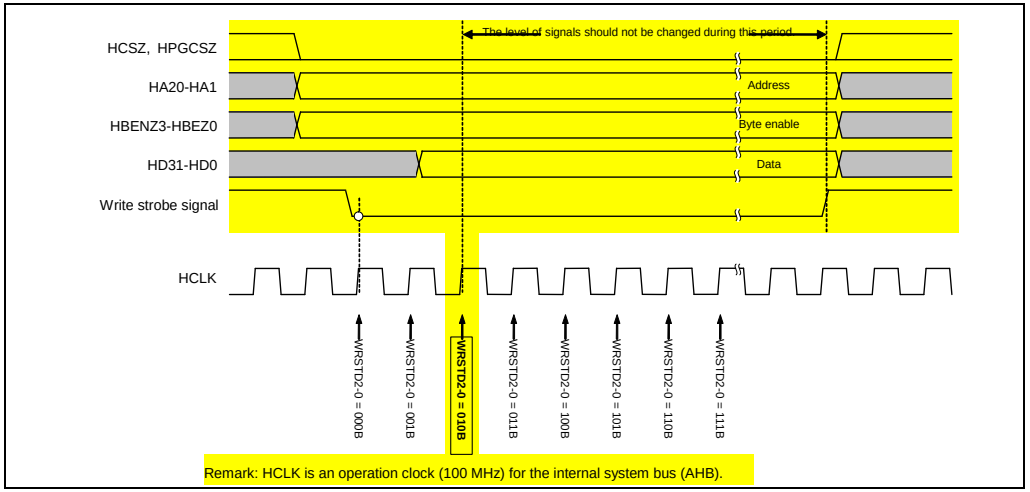
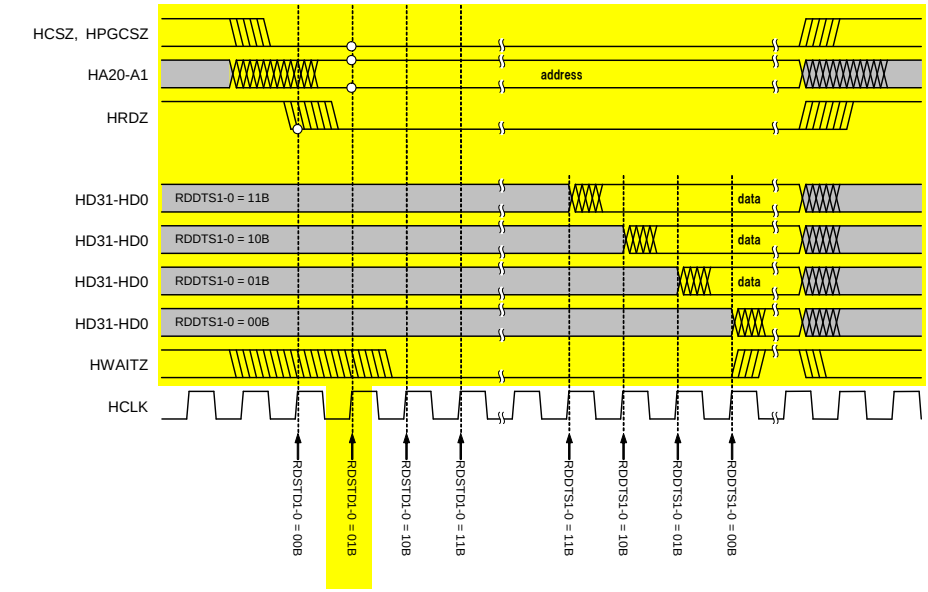


Figure 11.8 Timing Adjustment (SRAM writing)

16. 11.2.4(3) Timing adjustment (SRAM read, page ROM read)

"Figure 11.9 Timing Adjustment (SRAM read, page ROM read)", changed. (p.11-14)

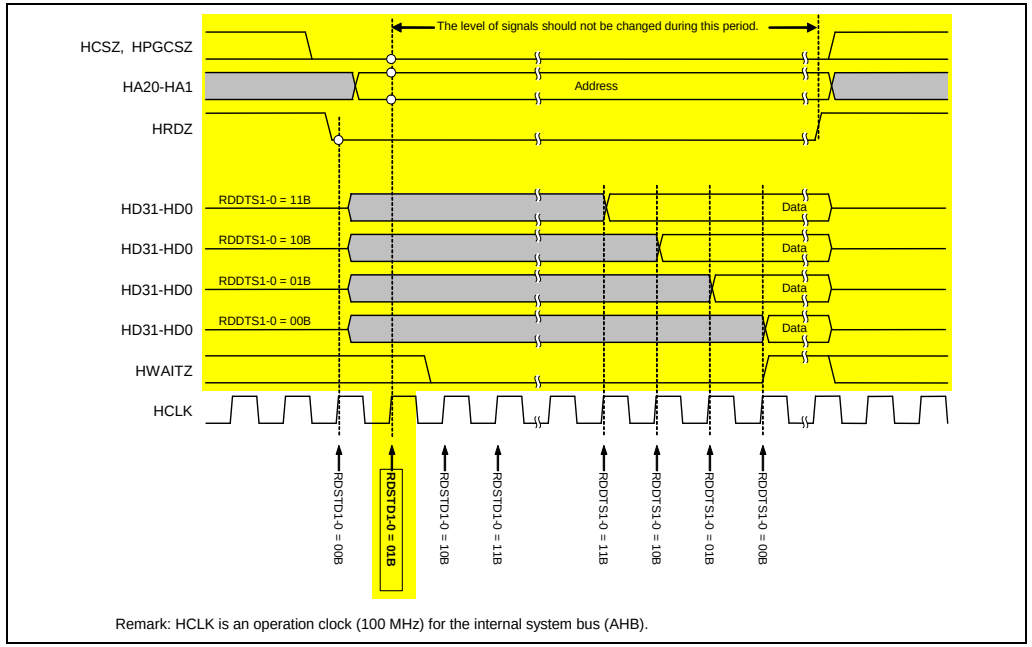
Rev7.00:



Remark : HCLK is a clock (100 MHz) of an internal system bus (AHB) of operation.

Figure 11.7 Timing Adjustment (SRAM read, page ROM read)

Rev8.00:



Remark: HCLK is an operation clock (100 MHz) for the internal system bus (AHB).

Figure 11.9 Timing Adjustment (SRAM read, page ROM read)

Caution: In reading of SRAM, input a stable address signal during bus cycles after the start of sampling. Input of an unstable address signal may create a possibility of incorrect data being read and completion of the bus cycle not being possible without the HWAITZ signal de-asserted.

17. 14.1 R-IN32M3 TAUJ2 Features

"Table14.3 TAUJ2 Interrupt signals", entry added to the table. (p.14-2)

Rev7.00:

Table14.3 TAUJ2 Interrupt signals

TAUJ2 signal	Function	Connected to
INTTAUJ2I0	Channel 0 interrupt	· Interrupt Controller INTTAUJ2I0 · DMA Controller trigger 0 (DTFR) · Timer Capture trigger 0 (TTFR) · Real-time Port trigger 0 (RPTFR)
INTTAUJ2I1	Channel 1 interrupt	· Interrupt Controller INTTAUJ2I1 · DMA Controller trigger 1 (DTFR) · Timer Capture trigger 1 (TTFR) · Real-time Port trigger 1 (RPTFR)
INTTAUJ2I2	Channel 2 interrupt	· Interrupt Controller INTTAUJ2I2 · DMA Controller trigger 2 (DTFR) · Timer Capture trigger 2 (TTFR) · Real-time Port trigger 2 (RPTFR)
INTTAUJ2I3	Channel 3 interrupt	· Interrupt Controller INTTAUJ2I3 · DMA Controller trigger 3 (DTFR) · Timer Capture trigger 3 (TTFR) · Real-time Port trigger 3 (RPTFR)

Rev8.00:

Table14.3 TAUJ2 Interrupt signals

TAUJ2 signal	Function	Connected to
INTTAUJ2I0	Channel 0 interrupt	· Interrupt Controller INTTAUJ2I0 · DMA Controller trigger (DTFR/RTDFTR) · Timer Capture trigger (TMTFR) · Real-time Port trigger (RPTFR) · HW-RTOS (Hardware ISR)
INTTAUJ2I1	Channel 1 interrupt	· Interrupt Controller INTTAUJ2I1 · DMA Controller trigger (DTFR/RTDFTR) · Timer Capture trigger (TMTFR) · Real-time Port trigger (RPTFR) · HW-RTOS (Hardware ISR)
INTTAUJ2I2	Channel 2 interrupt	· Interrupt Controller INTTAUJ2I2 · DMA Controller trigger (DTFR/RTDFTR) · Timer Capture trigger (TMTFR) · Real-time Port trigger (RPTFR) · HW-RTOS (Hardware ISR)
INTTAUJ2I3	Channel 3 interrupt	· Interrupt Controller INTTAUJ2I3 · DMA Controller trigger (DTFR/RTDFTR) · Timer Capture trigger (TMTFR) · Real-time Port trigger (RPTFR) · HW-RTOS (Hardware ISR)

* Applicable item except yellow hatched is unified description.

18. 14.1.1.1 Timer operation functions

“Table 14.4 TAUJ2 operation functions”, External Event Count Function added. (p.14-3)

Rev7.00:

Table 14.4 TAUJ2 operation functions

Independent channel operation function	Object item
Independent channel operation functions	
14.7.1「Interval Timer Function」	Interrupt is output every regular interval.
14.7.2「TAUJ2TTINm Input Interval Timer Function」	Interrupt is output by valid edge of every the regular internal or external input.
14.7.3「Delay Count Function」	The interrupt to which fixed delay was added is output to an effective input edge of external input.
14.7.4「TAUJ2TTINm Input Pulse Interval Measurement Function」	Time of the input space of the outside input signal is measured.
14.7.5「TAUJ2TTINm Input Signal Width Measurement Function」	The signal width of the outside input signal is measured.
Synchronous channel operation function	
14.8.1「PWM Output Function」	A corrugation is output.

Rev8.00:

Table 14.4 TAUJ2 operation functions

Independent channel operation function	Object item
Independent channel operation functions	
14.7.1 “Interval Timer Function”	Interrupts are output at regular intervals.
14.7.2 “TAUJ2TTINm Input Interval Timer Function”	Interrupts are output at regular intervals or when an effective edge of the external input signal is detected.
14.7.3 “Delay Count Function”	Interrupts which have a defined delay to the effective edge of the external input signal are output.
14.7.4 “TAUJ2TTINm Input Pulse Interval Measurement Function”	The interval of the external input signal is measured.
14.7.5 “TAUJ2TTINm Input Signal Width Measurement Function”	The signal width of the external input signal is measured.
14.7.6 “External Event Count Function”	This function is used as an event timer, which generates an interrupt in response to detection of the specified number of effective edges of the external input signal.
Synchronous channel operation function	
14.8.1 “PWM Output Function”	PWM waveform is output.

* Applicable item except yellow hatched is unified description.

19. 14.3.3(3) TAUJ2CMORm - TAUJ2 channel mode OS register
"Function" of TAUJ2CCS bit and TAUJ2MD bit, modified. (p.14-15 to 14-18)

Rev7.00:

(3) TAUJ2CMORm - TAUJ2 channel mode OS register

This register controls channel m operation.

● Access This register can be read or written in 16-bit units. Writing is only possible while the counter is stopped (TAUJ2TE.TAUJ2TEm = 0).

(1/4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TAUJ2 CMORm	TAUJ2 CKS[1:0]		TAUJ2 CCS[1:0]		TAUJ2MAS	TAUJ2STS [2:0]			TAUJ2 COS[1:0]		0	TAUJ2MD[4:0]					4000 0080H + m×4H	0000H
R/W	R/W		R/W		R/W	R/W			R/W		R	R/W						

Bit position	Bit name	Function
15, 14	TAUJ2CKS[1:0]	Selects the operation clock. The operation clock is used for the TAUJ2TTINm input edge detection circuit. It can also be used as the count clock depending on bits TAUJ2CMORm.CCS[1:0]. TAUJ2CKS1 / TAUJ2CKS0 / Selected prescaler output 0 / 0 / CK0 0 / 1 / CK1 1 / 0 / CK2 1 / 1 / CK3
13, 12	TAUJ2CCS[1:0]	Selects the count clock for TAUJ2CNTm counter. TAUJ2CCS1 / TAUJ2CCS0 / Selected count clock 0 / 0 / Prescaler output specified by TAUJ2CMORm.TAUJ2CKS[1:0] 1 / 0 / Setting prohibited 1 / 0 1 / 1
11	TAUJ2MAS	Specifies the channel as master or slave channel during synchronous channel operation. 0: Slave 1: Master This bit is only valid for even channels (CHm_even). For odd channels (CHm_odd), it is fixed to 0.

Rev8.00:

(3) TAUJ2CMORm - TAUJ2 channel mode OS register

This register controls channel m operation.

● Access This register can be read or written in 16-bit units. Writing is only possible while the counter is stopped (TAUJ2TE.TAUJ2TEm = 0).

(1/4)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
TAUJ2 CMORm	TAUJ2 CKS[1:0]		TAUJ2 CCS[1:0]		TAUJ2MAS	TAUJ2STS [2:0]			TAUJ2 COS[1:0]		0	TAUJ2MD[4:0]					4000 0080H + m×4H	0000H
R/W	R/W		R/W		R/W	R/W			R/W		R	R/W						

Bit position	Bit name	Function
15, 14	TAUJ2CKS[1:0]	Selects the operation clock. The operation clock is used for the TAUJ2TTINm input edge detection circuit. It can also be used as the count clock depending on bits TAUJ2CMORm.CCS[1:0]. TAUJ2CKS1 / TAUJ2CKS0 / Selected prescaler output 0 / 0 / CK0 0 / 1 / CK1 1 / 0 / CK2 1 / 1 / CK3
13, 12	TAUJ2CCS[1:0]	Selects the count clock for TAUJ2CNTm counter. TAUJ2CCS1 / TAUJ2CCS0 / Selected count clock 0 / 0 / Prescaler output specified by TAUJ2CMORm.TAUJ2CKS[1:0] 0 / 1 / Effective edge of TAUJ2TTINm input signal 1 / 0 / Setting prohibited 1 / 1
11	TAUJ2MAS	Specifies the channel as master or slave channel during synchronous channel operation. 0: Slave 1: Master This bit is only valid for even channels (CHm_even). For odd channels (CHm_odd), it is fixed to 0.

19. 14.3.3(3) TAUJ2CMORm - TAUJ2 channel mode OS register

"Function" of TAUJ2CCS bit and TAUJ2MD bit, modified. (p.14-15 to 14-18) continued

Rev7.00:

(4/4)

Bit position	Bit name	Function
5	—	Reserved
4-0	TAUJ2MD[4:0]	Specifies the operation mode.

TAUJ2 MD4	TAUJ2 MD3	TAUJ2 MD2	TAUJ2 MD1	TAUJ2 MD0	Description
0	0	0	0	1/0	Interval Timer mode
0	0	0	1	1/0	Setting prohibited
0	0	1	0	1/0	Capture mode
0	0	1	1	1/0	Setting prohibited
0	1	0	0	1/0	One Count mode
0	1	0	1	1/0	Setting prohibited
0	1	1	0	0	Capture & One Count mode
0	1	1	1	1/0	Setting prohibited
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1	1/0	Count Capture mode
1	1	0	0	1/0	Setting prohibited
1	1	0	1	0	Capture & Gate Count mode

Mode	Role of the MD0 bit
Interval Timer mode Capture mode Count Capture mode	Specifies whether the INTTAUJ2Im signal is output when the counter starts counting (when the start trigger is input). 0: Does not output INTTAUJ2Im. 1: Outputs INTTAUJ2Im
One Count mode	Enables/disables start trigger detection during counting: 0: Disables 1: Enables

Mode	Role of the MD0 bit
Capture & One Count mode Capture & Gate Count mode	This bit must be set to 0.

Rev8.00:

(4/4)

Bit position	Bit name	Function
5	—	Reserved
4-0	TAUJ2MD[4:0]	Specifies the operation mode.

TAUJ2 MD4	TAUJ2 MD3	TAUJ2 MD2	TAUJ2 MD1	TAUJ2 MD0	Description
0	0	0	0	1/0	Interval Timer mode
0	0	0	1	1/0	Setting prohibited
0	0	1	0	1/0	Capture mode
0	0	1	1	1/0	Event count mode
0	1	0	0	1/0	One Count mode
0	1	0	1	1/0	Setting prohibited
0	1	1	0	0	Capture & One Count mode
0	1	1	1	1/0	Setting prohibited
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1	1/0	Count Capture mode
1	1	0	0	1/0	Setting prohibited
1	1	0	1	0	Capture & Gate Count mode

Mode	Role of the MD0 bit
Interval Timer mode Capture mode Count Capture mode	Specifies whether the INTTAUJ2Im signal is output when the counter starts counting (when the start trigger is input). 0: Does not output INTTAUJ2Im. 1: Outputs INTTAUJ2Im
Event count mode	Set this bit to 0 (the NTTAUJ2Im signal is not output when the counter starts counting).
One Count mode	Enables/disables start trigger detection during counting: 0: Disables 1: Enables

Mode	Role of the MD0 bit
Capture & One Count mode Capture & Gate Count mode	This bit must be set to 0.

20. 14.7.6 External Event Count Function

“14.7.6 External Event Count Function”, added. (p.14-74 to 14-79)

Rev7.00:

No descriptions.

Rev8.00:

14.7.6 External Event Count Function

(1) Overview

(a) Summary

This function is used as an event timer, which generates an interrupt (INTTAUJ2Im) when the specified number of effective edges of the TAUJ2TTINm input signal are detected.

(b) Prerequisites

- The operating mode should be set to event count mode (see Table 14.36, Contents of the TAUJ2CMORm Register for External Event Count Function).
- TAUJ2TTOUTm is not used with this function.

(c) Functional description

The counter is enabled by setting the channel trigger bit (TAUJ2TS.TAUJ2TSm) to 1. This in turn sets TAUJ2TE.TAUJ2TEm = 1, enabling count operation. When the counter starts, the current value of TAUJ2CDRm is loaded into TAUJ2CNTm.
When an effective TAUJ2TTINm input edge is detected, the value of TAUJ2CNTm decrements by 1. TAUJ2CNTm retains this value until an effective TAUJ2TTINm input edge is detected or the counter is restarted.
When effective edges are detected (TAUJ2CDRm + 1) times, INTTAUJ2Im is generated. TAUJ2CNTm the loads the TAUJ2CDRm value and subsequently continues to operate.
The counter can be stopped by setting TAUJ2TT.TAUJ2TTm to 1, which in turn sets TAUJ2TE.TAUJ2TEm to 0. The counter can be restarted by setting TAUJ2TS.TAUJ2TSm to 1. The counter can also be restarted without stopping it first (forced restart) by setting TAUJ2TS.TAUJ2TSm to 1 during operation.
The value of TAUJ2CDRm can be rewritten at any time, and the changed value of TAUJ2CDRm is applied the next time the counter starts to count down.

(d) Conditions

The type of edge used as the trigger is specified by the TAUJ2CMURm.TAUJ2TIS[1:0] bits.

- When TAUJ2CMURm.TAUJ2TIS[1:0] = 00B, falling edges trigger the counter.
- When TAUJ2CMURm.TAUJ2TIS[1:0] = 01B, rising edges trigger the counter.
- When TAUJ2CMURm.TAUJ2TIS[1:0] = 10B, rising and falling edges trigger the counter.

(2) Equations

Number of effective edges detected before INTTAUJ2Im is generated = TAUJ2CDRm + 1

20. 14.7.6 External Event Count Function

“14.7.6 External Event Count Function”, added. (p.14-74 to 14-79) continued

Rev7.00:

No descriptions.

Rev8.00:

(3) Block diagram and general timing diagram

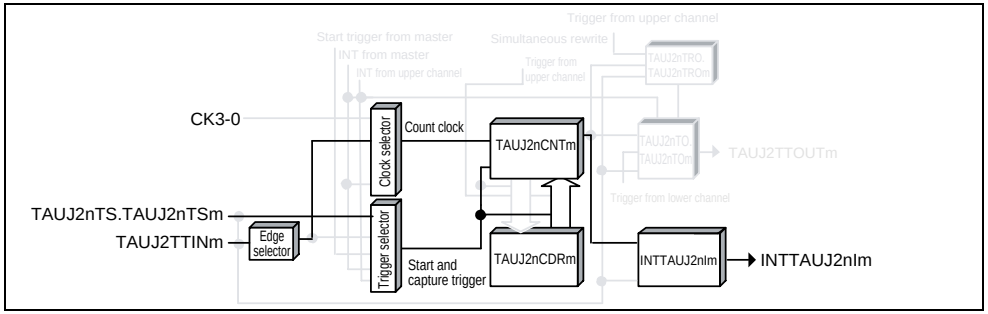


Figure 14.26 Block Diagram of External Event Count Function

The following settings apply to the general timing diagram.
•Detection of rising edges (TAUJ2CMURm.TAUJ2TIS[1:0] = 01B)

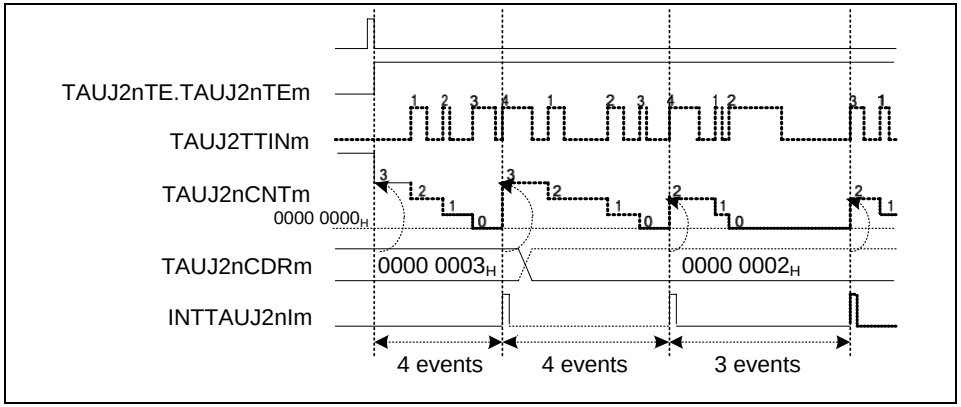


Figure 14.27 General Timing Diagram of External Event Count Function

20. 14.7.6 External Event Count Function

“14.7.6 External Event Count Function”, added. (p.14-74 to 14-79) continued

Rev7.00:

No descriptions.

Rev8.00:

(4) Register settings

(a) TAUJ2CMORm

15 14	13 12	11	10 9 8	7 6	5	4 3 2 1	0
TAUJ2CKS [1:0]	TAUJ2CCS [1:0]	TAUJ2 MAS	TAUJ2STS [2:0]	TAUJ2COS [1:0]	0	TAUJ2MD[4:1]	TAUJ2MD0

Table 14.36 Contents of the TAUJ2CMORm Register for External Event Count Function

Bit name	Setting
TAUJ2CKS[1:0]	Operation Clock Selection 00: Prescaler output = CK0 01: Prescaler output = CK1 10: Prescaler output = CK2 11: Prescaler output = CK3
TAUJ2CCS[1:0]	01: Effective TAUJ2TTINm input edge is used as a counter clock.
TAUJ2MAS	0: Independent operation. Set to 0.
TAUJ2STS[2:0]	000: Trigger the counter using software.
TAUJ2COS[1:0]	00: Unused. Set to 00.
TAUJ2MD[4:1]	0011: Event count mode.
TAUJ2MD0	0: INTTAUJ2Im not generated at the beginning of operation.

(b) TAUJ2CMURm

7	6	5	4	3	2	1 0
0	0	0	0	0	0	TAUJ2TIS[1:0]

Table 14.37 Contents of the TAUJ2CMURm Register for External Event Count Function

Bit name	Setting
TAUJ2TIS[1:0]	00: Detection of falling edges 01: Detection of rising edges 10: Detection of falling and rising edges

(c) Channel output mode

The channel output mode is not used by this function.

20. 14.7.6 External Event Count Function

“14.7.6 External Event Count Function”, added. (p.14-74 to 14-79) continued

Rev7.00:

No descriptions.

Rev8.00:

(d) Simultaneous rewrite

Simultaneous rewrite registers (TAUJ2RDE, TAUJ2RDS, TAUJ2RDM, and TAUJ2RDC) cannot be used with this function. Therefore, these registers should be set to 0.

Table 14.38 Simultaneous Rewrite Settings for External Event Count Function

Bit name	Setting
TAUJ2RDE.TAUJ2RDEm	0: Disables simultaneous rewrite
TAUJ2RDS.TAUJ2RDSm	0: When simultaneous rewrite is disabled (TAUJ2RDE.TAUJ2RDEm = 0), set these bits to 0.
TAUJ2RDM.TAUJ2RDMm	
TAUJ2RDC.TAUJ2RDCm	

(5) Operating Procedure for External Event Count Function

Table 14.39 Operating Procedure for External Event Count Function

	Operation	Status of TAUJ2
Initial channel setting	Set TAUJ2CMORm and TAUJ2CMURm registers as described in, Table 14.36, Contents of the TAUJ2CMORm Register for External Event Count Function and Table 14.37, Contents of the TAUJ2CMURm Register for External Event Count Function. Set the value of TAUJ2CDRm register.	Channel operation is stopped.
Start operation	Set TAUJ2TS.TAUJ2TSm to 1. TAUJ2TS.TAUJ2TSm is a trigger bit, so it is automatically cleared to 0.	TAUJ2TE.TAUJ2TEm is set to 1 and the counter starts. TAUJ2CNTm loads the TAUJ2CDRm value and waits for detection of the TAUJ2TTINm input edge.
During operation	Detection of TAUJ2TTINm edges The value of TAUJ2CDRm can be changed at any time. The TAUJ2CNTm register can be read at any time.	TAUJ2CNTm counts down each time a TAUJ2TTINm input edge is detected. When the counter reaches 0000H: •TAUJ2CNTm loads the TAUJ2CDRm value and continues counting. •INTTAUJ2Im is generated. Afterwards, this procedure is repeated.
Stop operation	Set TAUJ2TT.TAUJ2TTm to 1. TAUJ2TT.TAUJ2TTm is a trigger bit, so it is automatically cleared to 0.	TAUJ2TE.TAUJ2TEm is cleared to 0 and the counter stops. TAUJ2CNTm stops and retains its current value.

Restart

20. 14.7.6 External Event Count Function

"14.7.6 External Event Count Function", added. (p.14-74 to 14-79) continued

Rev7.00:

No descriptions.

Rev8.00:

(6) Specific timing diagrams

(a) TAUJ2CDRm = 0000 0000H

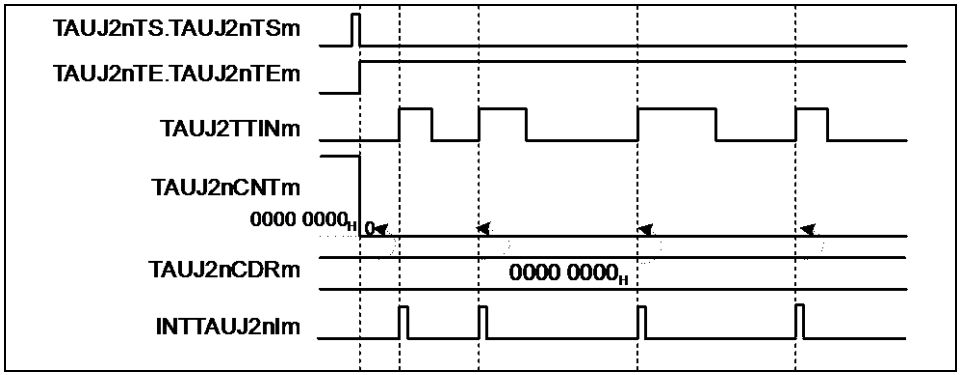


Figure 14.28 TAUJ2CDRm = 0000 0000H, TAUJ2CMURm.TAUJ2TIS[1:0] = 01B

- If 0000 0000H = TAUJ2CDRm, 0000 0000H is loaded to TAUJ2CNTm every time an effective TAUJ2TTINm input edge is detected. In other words, INTTAUJ2Im is generated every time an effective TAUJ2TTINm input edge is detected.

(b) Operation stop and restart

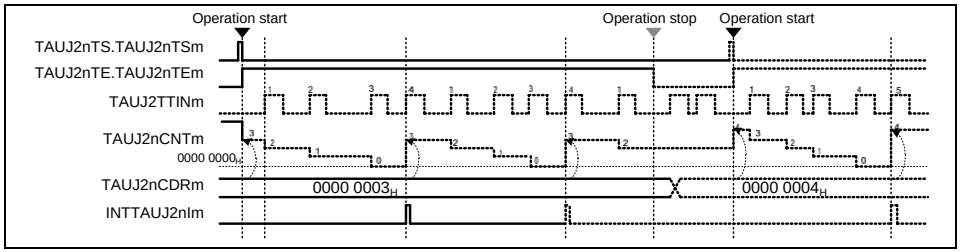


Figure 14.29 Operation Stop and Restart (TAUJ2CMURm.TAUJ2TIS[1:0] = 01B)

- The counter can be stopped by setting TAUJ2TT.TAUJ2TTm to 1. This in turn sets TAUJ2TE.TAUJ2TEm to 0.
- TAUJ2CNTm stops and retains its current value. TAUJ2TTINm continues and TAUJ2CNTm ignores the effective edge.
- The counter can be restarted by setting TAUJ2TS.TAUJ2TSm to 1. TAUJ2CNTm loads the TAUJ2CDRm value and restarts counting.

20. 14.7.6 External Event Count Function

“14.7.6 External Event Count Function”, added. (p.14-74 to 14-79) continued

Rev7.00:

No descriptions.

Rev8.00:

(c) Forced restart

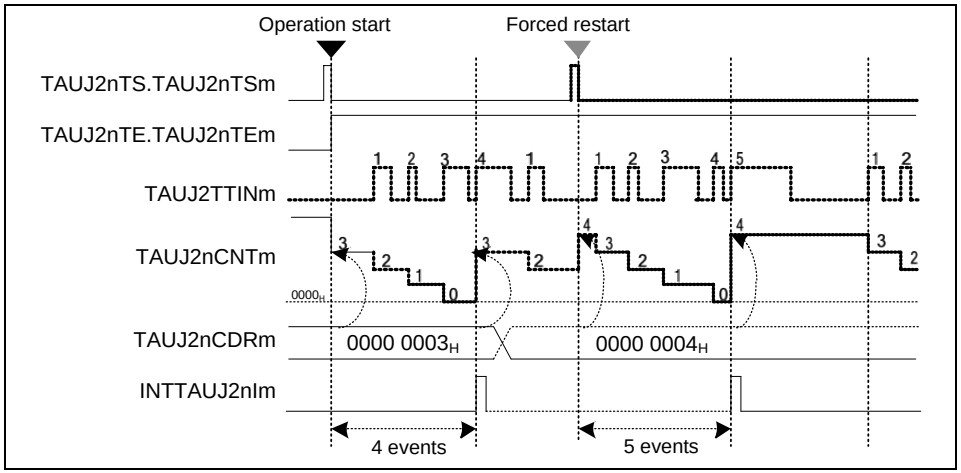


Figure 14.30 Forced Restart (TAUJ2CMURm.TAUJ2TIS[1:0] = 01B)

Once a forced restart is made, the changed TAUJ2CDRm value is applied to TAUJ2CNTm immediately.

- The counter can be restarted without making a stop by setting TAUJ2TS.TAUJ2TSm to 1 during operation.
- The value of TAUJ2CDRm is loaded into TAUJ2CNTm and the counter awaits the next effective TAUJ2TTINm input edge.

21. 15.3.2(2) WDTA Mode Register (WDTAnMD)
“Bit Name” of WDTAn*** unified to WDTA0***. (p.15-4)

Rev7.00:

(2) WDTA Mode Register (WDTAnMD)

This register specifies the overflow interval time, error mode, and open window size.

It can be updated only once after release from the reset state and before the first trigger. The updated value is effective from the next WDTA trigger.

Changing the value of this register after WDTA has been started leads to an error, but writing the same value to it does not generate an error.

- Access This register can be read/written in 8-bit units.

	7	6	5	4	3	2	1	0	Address	Initial Value
WDTA0MD	0	WDTAnOVF[2:0]			0	WDTAnERM	WDTAnWS[1:0]		4000 070CH	0FH
R/W	0	R/W			0	R/W	R/W			

Bit Position	Bit Name	Description
7	–	Reserved. Writing 0 has no effect. When read, 0 is returned.
6-4	WDTAnOVF[2:0]	Selects the overflow interval time:
3	–	Reserved
2	WDTAnERM	Specifies the error mode: 0: NMI request mode 1: Reset mode
1,0	WDTAnWS[1:0]	Select the open window size:

WDTAnOVF2	WDTAnOVF1	WDTAnOVF0	Overflow interval time
0	0	0	2^9 / WDTATCKI
0	0	1	2^{10} / WDTATCKI
0	1	0	2^{11} / WDTATCKI
0	1	1	2^{12} / WDTATCKI
1	0	0	2^{13} / WDTATCKI
1	0	1	2^{14} / WDTATCKI
1	1	0	2^{15} / WDTATCKI
1	1	1	2^{16} / WDTATCKI

WDTAnWS1	WDTAnWS0	Open window size
0	0	25%
0	1	50%
1	0	75%
1	1	100%

Rev8.00:

(2) WDTA Mode Register (WDTAnMD)

This register specifies the overflow interval time, error mode, and open window size.

It can be updated only once after release from the reset state and before the first trigger. The updated value is effective from the next WDTA trigger.

Changing the value of this register after WDTA has been started leads to an error, but writing the same value to it does not generate an error.

- Access This register can be read/written in 8-bit units.

	7	6	5	4	3	2	1	0	Address	Initial Value
WDTA0MD	0	WDTA0OVF[2:0]			0	WDTA0ERM	WDTA0WS[1:0]		4000 070CH	0FH
R/W	0	R/W			0	R/W	R/W			

Bit Position	Bit Name	Description
7	–	Reserved. Writing 0 has no effect. When read, 0 is returned.
6-4	WDTA0OVF[2:0]	Selects the overflow interval time:
3	–	Reserved
2	WDTA0ERM	Specifies the error mode: 0: NMI request mode 1: Reset mode
1,0	WDTA0WS[1:0]	Select the open window size:

WDTA0OVF2	WDTA0OVF1	WDTA0OVF0	Overflow interval time
0	0	0	2^9 / WDTATCKI
0	0	1	2^{10} / WDTATCKI
0	1	0	2^{11} / WDTATCKI
0	1	1	2^{12} / WDTATCKI
1	0	0	2^{13} / WDTATCKI
1	0	1	2^{14} / WDTATCKI
1	1	0	2^{15} / WDTATCKI
1	1	1	2^{16} / WDTATCKI

WDTA0WS1	WDTA0WS0	Open window size
0	0	25%
0	1	50%
1	0	75%
1	1	100%

22. 17.1 R-IN32M3 CSIH Features

"Table 17.5 CSIHn Interrupt and DMA/DTS requests", entry added to the table. (p.17-2)

Rev7.00:

Table 17.5 CSIHn Interrupt and DMA/DTS requests

CSIHn signals	Function	Connected to
CSIH0		
CSIHTIC	Communication interrupt	・Interrupt controller (INTCSIH0IC) ・DMA controller trigger C (DTFR) ・Timer Capture trigger C (TTFR) ・Real Time port trigger C (RPTFR)
CSIHTIR	Reception interrupt	・Interrupt controller (INTCSIH0IR) ・DMA controller trigger D ・Timer Capture trigger D (TTFR) ・Real Time port trigger D (RPTFR)
CSIHTIRE	Reception error interrupt	・Interrupt controller (INTCSIH0IRE)
CSIHTIJC	Job completion interrupt	・Interrupt controller (INTCSIH0IJC) ・DMA controller trigger E (DTFR) ・Timer Capture trigger E (TTFR) ・Real Time port trigger E (RPTFR)
CSIH1		
CSIHTIC	Communication interrupt	・Interrupt controller (INTCSIH1IC) ・DMA controller trigger F (DTFR) ・Timer Capture trigger F (TTFR) ・Real Time port trigger F (RPTFR)
CSIHTIR	Reception interrupt	・Interrupt controller (INTCSIH1IR) ・DMA controller trigger 10 (DTFR) ・Timer Capture trigger 10 (TTFR) ・Real Time port trigger 10 (RPTFR)
CSIHTIRE	Reception error interrupt	・Interrupt controller (INTCSIH1IRE)
CSIHTIJC	Job completion interrupt	・Interrupt controller (INTCSIH1IJC) ・DMA controller trigger 11 (DTFR) ・Timer Capture trigger 11 (TTFR) ・Real Time port trigger 11 (RPTFR)

Rev8.00:

Table 17.5 CSIHn Interrupt and DMA/DTS requests

CSIHn signals	Function	Connected to
CSIH0		
CSIHTIC	Communication interrupt	・Interrupt controller (INTCSIH0IC) ・DMA controller trigger (DTFR/RTDFTR) ・Timer Capture trigger (TMTFR) ・Real Time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
CSIHTIR	Reception interrupt	・Interrupt controller (INTCSIH0IR) ・DMA controller trigger (DTFR/RTDFTR) ・Timer Capture trigger (TMTFR) ・Real Time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
CSIHTIRE	Reception error interrupt	・Interrupt controller (INTCSIH0IRE) ・HW-RTOS (Hardware ISR)
CSIHTIJC	Job completion interrupt	・Interrupt controller (INTCSIH0IJC) ・DMA controller trigger (DTFR/RTDFTR) ・Timer Capture trigger (TMTFR) ・Real Time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
CSIH1		
CSIHTIC	Communication interrupt	・Interrupt controller (INTCSIH1IC) ・DMA controller trigger (DTFR/RTDFTR) ・Timer Capture trigger (TMTFR) ・Real Time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
CSIHTIR	Reception interrupt	・Interrupt controller (INTCSIH1IR) ・DMA controller trigger (DTFR/RTDFTR) ・Timer Capture trigger (TMTFR) ・Real Time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
CSIHTIRE	Reception error interrupt	・Interrupt controller (INTCSIH1IRE) ・HW-RTOS (Hardware ISR)
CSIHTIJC	Job completion interrupt	・Interrupt controller (INTCSIH1IJC) ・DMA controller trigger (DTFR/RTDFTR) ・Timer Capture trigger (TMTFR) ・Real Time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)

* Applicable item except yellow hatched is unified description.

23. 18.9.1(3) Master operate setting sequence during continuous transfer mode

"Figure 18.16 Master operate setting sequence during continuous transfer mode (single master environment)", modified. (p.18-120)

Rev7.00:

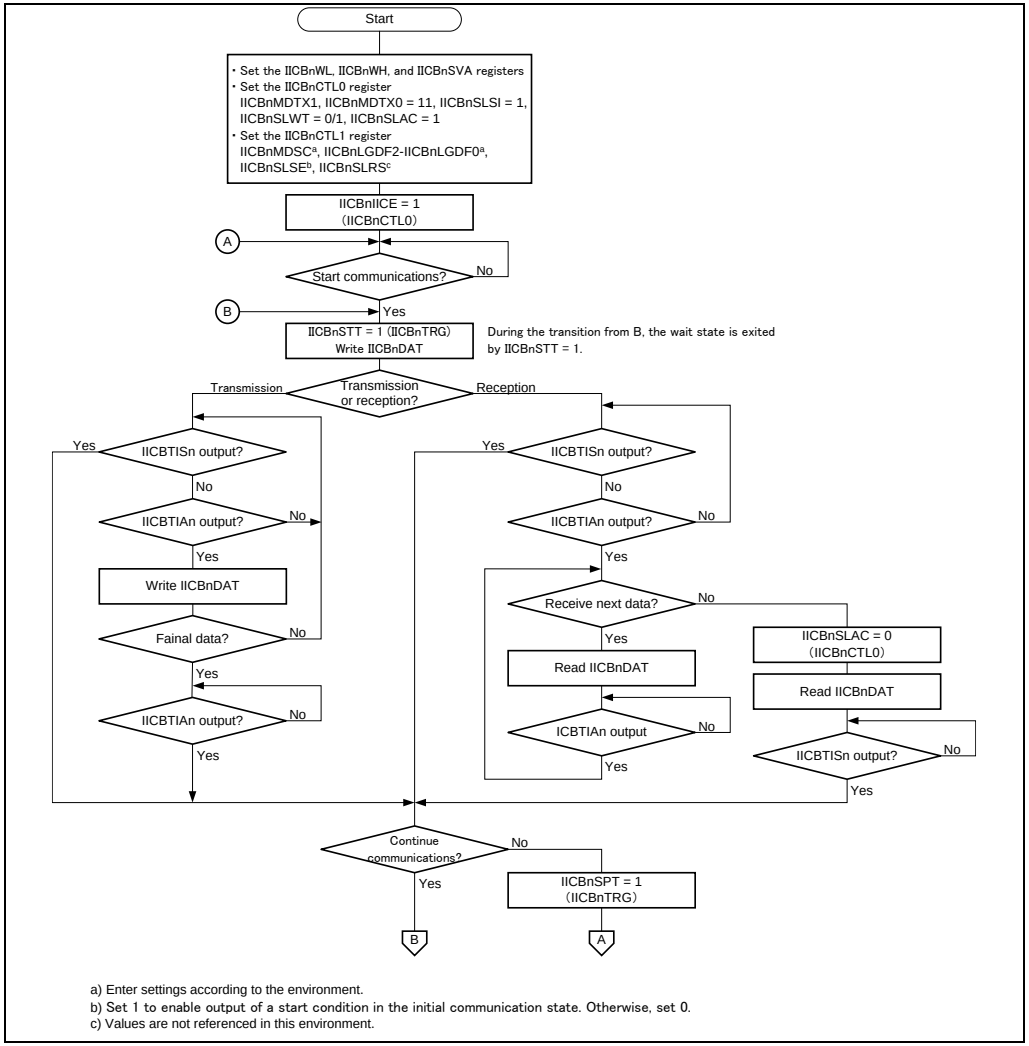


Figure 18.16 Master operate setting sequence during continuous transfer mode (single master environment)

Rev8.00:

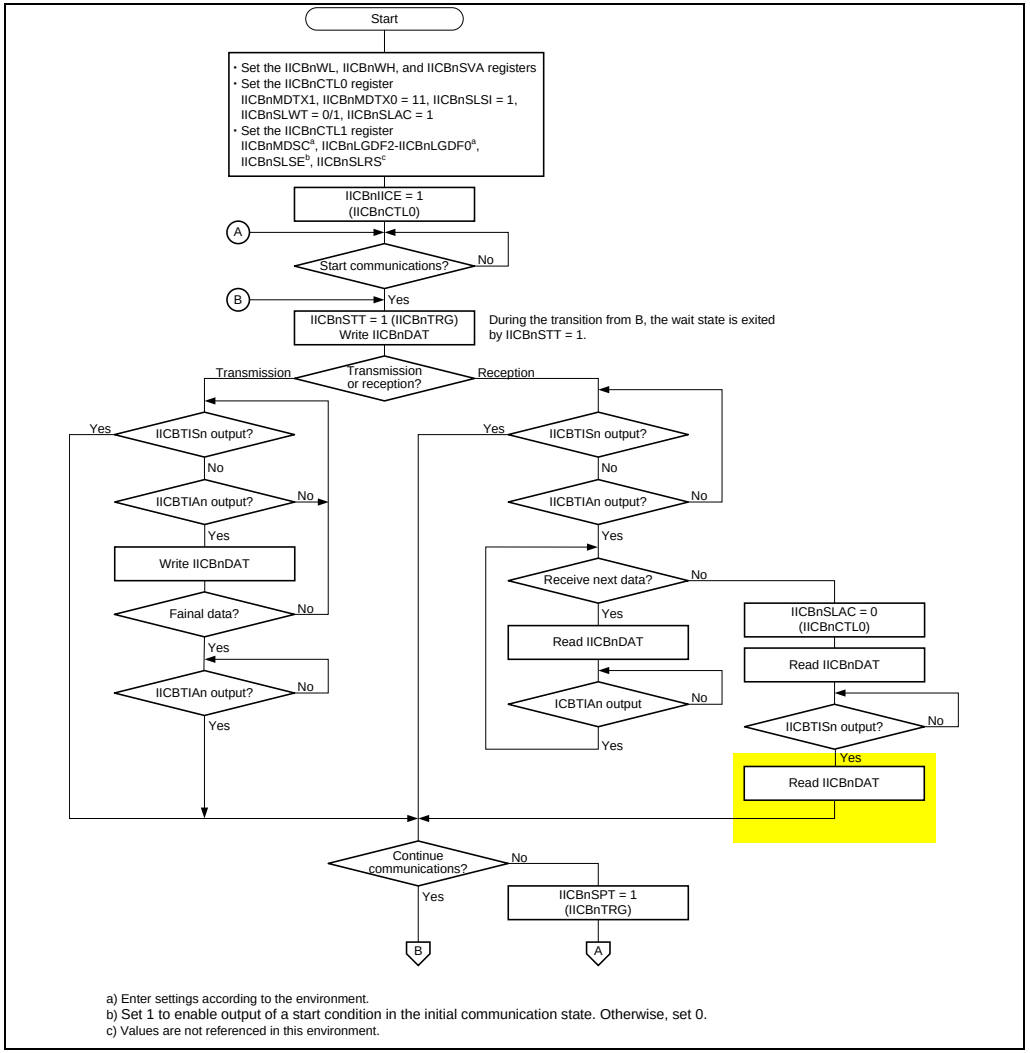


Figure 18.16 Master operate setting sequence during continuous transfer mode (single master environment)

24. 19.1 FCN Features of R-IN32M3

"Table 19.4 FCNn interrupts and DMA requests", entry added to the table. (p.19-114)

Rev7.00:

Table 19.4 FCNn interrupts and DMA requests

FCNn Interrupt	Function	Connected to
FCN0		
INTC0ERR	FCN0 error detected	・Interrupt controller INTFCN0ERR
INTC0REC	FCN0 reception completion	・Interrupt controller INTFCN0REC ・DMA controller trigger 14 (DTFR) ・timers capture trigger 14 (TTFR) ・realtime port trigger 14 (RPTFR)
INTC0TRX	FCN0 transmission completion	・Interrupt controller INTFCN0TRX ・DMA controller trigger 15 (DTFR) ・timers capture trigger 15 (TTFR) ・realtime port trigger 15 (RPTFR)
INTC0WUP	FCN0 sleep wake-up / transmission abortion	・Interrupt controller INTFCN0WUP ・DMA controller trigger 16 (DTFR) ・timers capture trigger 16 (TTFR) ・realtime port trigger 16 (RPTFR)
FCN1		
INTC1ERR	FCN1 error detected	・Interrupt controller INTFCN1ERR
INTC1REC	FCN1 reception completion	・Interrupt controller INTFCN1REC ・DMA controller trigger 17 (DTFR) ・timers capture trigger 17 (TTFR) ・realtime port trigger 17 (RPTFR)
INTC1TRX	FCN1 transmission completion	・Interrupt controller INTFCN1TRX ・DMA controller trigger 18 (DTFR) ・timers capture trigger 18 (TTFR) ・realtime port trigger 18 (RPTFR)
INTC1WUP	FCN1 sleep wake-up / transmission abortion	・Interrupt controller INTFCN1WUP ・DMA controller trigger 19 (DTFR) ・timers capture trigger 19 (TTFR) ・realtime port trigger 19 (RPTFR)

Rev8.00:

Table 19.4 FCNn interrupts and DMA requests

FCNn Interrupt	Function	Connected to
FCN0		
INTC0ERR	FCN0 error detected	・Interrupt controller INTFCN0ERR ・HW-RTOS (Hardware ISR)
INTC0REC	FCN0 reception completion	・Interrupt controller INTFCN0REC ・DMA controller trigger (DTFR/RTDTFR) ・timers capture trigger (TMTFR) ・Real-time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
INTC0TRX	FCN0 transmission completion	・Interrupt controller INTFCN0TRX ・DMA controller trigger (DTFR/RTDTFR) ・timers capture trigger (TMTFR) ・Real-time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
INTC0WUP	FCN0 sleep wake-up / transmission abortion	・Interrupt controller INTFCN0WUP ・DMA controller trigger (DTFR/RTDTFR) ・timers capture trigger (TMTFR) ・Real-time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
FCN1		
INTC1ERR	FCN1 error detected	・Interrupt controller INTFCN1ERR ・HW-RTOS (Hardware ISR)
INTC1REC	FCN1 reception completion	・Interrupt controller INTFCN1REC ・DMA controller trigger (DTFR/RTDTFR) ・timers capture trigger (TMTFR) ・Real-time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
INTC1TRX	FCN1 transmission completion	・Interrupt controller INTFCN1TRX ・DMA controller trigger (DTFR/RTDTFR) ・timers capture trigger (TMTFR) ・Real-time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)
INTC1WUP	FCN1 sleep wake-up / transmission abortion	・Interrupt controller INTFCN1WUP ・DMA controller trigger (DTFR/RTDTFR) ・timers capture trigger (TMTFR) ・Real-time port trigger (RPTFR) ・HW-RTOS (Hardware ISR)

* Applicable item except yellow hatched is unified description.

25. 19.13.2 Representative examples of baud rate settings

"Table 19.20 Representative examples of baud rate settings", title and entries in the table modified. (p.19-114)

Rev7.00:

Table 19.20 Representative examples of baud rate settings (f_{CANMOD} = 25MHz) (1/2)

Set baud rate value (unit: kbps)	Division ratio of FCNnCMB RPRS register	FCNnCMB RPRS register set value	Valid bit rate setting (unit: TQ)					FCNnCMBTCTL register setting value		Sampling point (unit: %)
			Length of DBT	SYNC SEGMENT	PROP SEGMENT	PHASE SEGMENT1	PHASE SEGMENT2	FCNnCMB TS1LG[3:0]	FCNnCMB TS2LG[2:0]	
1000	1	00000000	20	1	3	8	8	1010	111	60.0
1000	1	00000000	20	1	5	7	7	1011	110	65.0
1000	1	00000000	20	1	7	6	6	1100	101	70.0
1000	1	00000000	20	1	7	4	4	1101	100	75.0
1000	1	00000000	20	1	9	5	5	1110	011	80.0
1000	1	00000000	20	1	11	2	2	1111	010	85.0
1000	2	00000001	10	1	1	4	4	0100	011	60.0
1000	2	00000001	10	1	3	3	3	0101	010	70.0
1000	2	00000001	10	1	5	2	2	0110	001	80.0
1000	2	00000001	10	1	7	1	1	0111	000	90.0
500	2	00000001	20	1	3	8	8	1010	111	60.0
500	2	00000001	20	1	5	7	7	1011	110	65.0
500	2	00000001	20	1	7	6	6	1100	101	70.0
500	2	00000001	20	1	7	4	4	1101	100	75.0
500	2	00000001	20	1	9	5	5	1110	011	80.0
500	2	00000001	20	1	11	2	2	1111	010	85.0
500	4	00000011	10	1	1	4	4	0100	011	60.0
500	4	00000011	10	1	3	3	3	0101	010	70.0
500	4	00000011	10	1	5	2	2	0110	001	80.0
500	4	00000011	10	1	7	1	1	0111	000	90.0
250	4	00000011	20	1	5	7	7	1011	110	65.0
250	4	00000011	20	1	7	6	6	1100	101	70.0
250	4	00000011	20	1	9	5	5	1101	100	75.0
250	4	00000011	20	1	11	4	4	1110	011	80.0
250	8	00000111	10	1	3	3	3	0101	010	70.0
250	8	00000111	10	1	5	2	2	0110	001	80.0
125	8	00000111	20	1	5	7	7	1011	110	65.0
125	8	00000111	20	1	7	6	6	1100	101	70.0
125	8	00000111	20	1	9	5	5	1101	100	75.0
125	8	00000111	20	1	11	4	4	1110	011	80.0
125	16	00001111	10	1	3	3	3	0101	010	70.0
125	16	00001111	10	1	5	2	2	0110	001	80.0
100	10	00001001	20	1	5	7	7	1011	110	65.0
100	10	00001001	20	1	7	6	6	1100	101	70.0
100	10	00001001	20	1	7	4	4	1101	100	75.0
100	10	00001001	20	1	9	5	5	1110	011	80.0
100	20	00010011	10	1	3	3	3	0101	010	70.0
100	20	00010011	10	1	5	2	2	0110	001	80.0

Rev8.00:

Table 19.20 Representative examples of baud rate settings (f_{CANMOD} = 20MHz) (1/2)

Set baud rate value (unit: kbps)	Division ratio of FCNnCMB RPRS register	FCNnCMB RPRS register set value	Valid bit rate setting (unit: TQ)					FCNnCMBTCTL register setting value		Sampling point (unit: %)
			Length of DBT	SYNC SEGMENT	PROP SEGMENT	PHASE SEGMENT1	PHASE SEGMENT2	FCNnCMB TS1LG[3:0]	FCNnCMB TS2LG[2:0]	
1000	1	00000000	20	1	3	8	8	1010	111	60.0
1000	1	00000000	20	1	5	7	7	1011	110	65.0
1000	1	00000000	20	1	7	6	6	1100	101	70.0
1000	1	00000000	20	1	7	4	4	1101	100	75.0
1000	1	00000000	20	1	9	5	5	1110	011	80.0
1000	1	00000000	20	1	11	4	4	1111	010	85.0
1000	2	00000001	10	1	1	4	4	0100	011	60.0
1000	2	00000001	10	1	3	3	3	0101	010	70.0
1000	2	00000001	10	1	5	2	2	0110	001	80.0
1000	2	00000001	10	1	7	1	1	0111	000	90.0
500	2	00000001	20	1	3	8	8	1010	111	60.0
500	2	00000001	20	1	5	7	7	1011	110	65.0
500	2	00000001	20	1	7	6	6	1100	101	70.0
500	2	00000001	20	1	7	4	4	1101	100	75.0
500	2	00000001	20	1	9	5	5	1110	011	80.0
500	2	00000001	20	1	11	4	4	1111	010	85.0
500	4	00000011	10	1	1	4	4	0100	011	60.0
500	4	00000011	10	1	3	3	3	0101	010	70.0
500	4	00000011	10	1	5	2	2	0110	001	80.0
500	4	00000011	10	1	7	1	1	0111	000	90.0
250	4	00000011	20	1	5	7	7	1011	110	65.0
250	4	00000011	20	1	7	6	6	1100	101	70.0
250	4	00000011	20	1	9	5	5	1101	100	75.0
250	4	00000011	20	1	11	4	4	1110	011	80.0
250	8	00000111	10	1	3	3	3	0101	010	70.0
250	8	00000111	10	1	5	2	2	0110	001	80.0
125	8	00000111	20	1	5	7	7	1011	110	65.0
125	8	00000111	20	1	7	6	6	1100	101	70.0
125	8	00000111	20	1	9	5	5	1101	100	75.0
125	8	00000111	20	1	11	4	4	1110	011	80.0
125	16	00001111	10	1	3	3	3	0101	010	70.0
125	16	00001111	10	1	5	2	2	0110	001	80.0
100	10	00001001	20	1	5	7	7	1011	110	65.0
100	10	00001001	20	1	7	6	6	1100	101	70.0
100	10	00001001	20	1	7	4	4	1101	100	75.0
100	10	00001001	20	1	9	5	5	1110	011	80.0
100	20	00010011	10	1	3	3	3	0101	010	70.0
100	20	00010011	10	1	5	2	2	0110	001	80.0

26. 21.1 Registers

CPUBUSMD register added. (p.21-2)

Rev7.00:

Register Name	Symbol	Address	Protection	Access bit unit		Access by external MCU
				16	32	
Scratch register 0	SCRATCH0	BASE+0900H		√	√	√
Scratch register 1	SCRATCH1	BASE+0904H		√	√	√
Scratch register 2	SCRATCH2	BASE+0908H		√	√	√
Scratch register 3	SCRATCH3	BASE+090CH		√	√	√
Scratch register 4	SCRATCH4	BASE+0910H		√	√	√
Scratch register 5	SCRATCH5	BASE+0914H		√	√	√
Scratch register 6	SCRATCH6	BASE+0918H		√	√	√
Scratch register 7	SCRATCH7	BASE+091CH		√	√	√
Scratch register 8	SCRATCH8	BASE+0920H		√	√	√
Scratch register 9	SCRATCH9	BASE+0924H		√	√	√
Scratch register A	SCRATCHA	BASE+0928H		√	√	√
Scratch register B	SCRATCHB	BASE+092CH		√	√	√
Scratch register C	SCRATCHC	BASE+0930H		√	√	√
Scratch register D	SCRATCHD	BASE+0934H		√	√	√
Trigger-synchronous port control mode register	RPTRGMD	BASE+0A00H	√		√	
Trigger-synchronous port source register 0	RP0TFR	BASE+0A30H	√		√	
Trigger-synchronous port source register 1	RP1TFR	BASE+0A34H	√		√	
Trigger-synchronous port source register 2	RP2TFR	BASE+0A38H	√		√	
Trigger-synchronous port source register 3	RP3TFR	BASE+0A3CH	√		√	

Rev8.00:

Register Name	Symbol	Address	Protection	Access bit unit		Access by external MCU
				16	32	
Scratch register 0	SCRATCH0	BASE+0900H		√	√	√
Scratch register 1	SCRATCH1	BASE+0904H		√	√	√
Scratch register 2	SCRATCH2	BASE+0908H		√	√	√
Scratch register 3	SCRATCH3	BASE+090CH		√	√	√
Scratch register 4	SCRATCH4	BASE+0910H		√	√	√
Scratch register 5	SCRATCH5	BASE+0914H		√	√	√
Scratch register 6	SCRATCH6	BASE+0918H		√	√	√
Scratch register 7	SCRATCH7	BASE+091CH		√	√	√
Scratch register 8	SCRATCH8	BASE+0920H		√	√	√
Scratch register 9	SCRATCH9	BASE+0924H		√	√	√
Scratch register A	SCRATCHA	BASE+0928H		√	√	√
Scratch register B	SCRATCHB	BASE+092CH		√	√	√
Scratch register C	SCRATCHC	BASE+0930H		√	√	√
Scratch register D	SCRATCHD	BASE+0934H		√	√	√
Trigger-synchronous port control mode register	RPTRGMD	BASE+0A00H	√		√	
Trigger-synchronous port source register 0	RP0TFR	BASE+0A30H	√		√	
Trigger-synchronous port source register 1	RP1TFR	BASE+0A34H	√		√	
Trigger-synchronous port source register 2	RP2TFR	BASE+0A38H	√		√	
Trigger-synchronous port source register 3	RP3TFR	BASE+0A3CH	√		√	
CPU bus mode register	CPUBUSMD	BASE+0214H		√	√	√

27. 21.4 Version register (RINVER)

“Initial Value” of RINVER register, modified. Remark added. (p.21-4)

Rev7.00:

21.4 Version register (RINVER)

This register is used to identify the version of the R-IN32M3.
If read, 0000 0001H is returned. Access This register can be read in 32-bit or 16-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RINVER	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	BASE +0008H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Initial Value 0000 0001H

Rev8.00:

21.4 Version register (RINVER)

This register is used to identify the version of an R-IN32M3. If read, 0000 0002H is returned.

- Access: This register can be read in 32- or 16-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RINVER	RINVER31	RINVER30	RINVER29	RINVER28	RINVER27	RINVER26	RINVER25	RINVER24	RINVER23	RINVER22	RINVER21	RINVER20	RINVER19	RINVER18	RINVER17	RINVER16	RINVER15	RINVER14	RINVER13	RINVER12	RINVER11	RINVER10	RINVER9	RINVER8	RINVER7	RINVER6	RINVER5	RINVER4	RINVER3	RINVER2	RINVER1	RINVER1	BASE +0008H
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial Value 0000 0002H

Bit Position	Bit Name	Description
31 to 0	RINVER31-0	These bits are for identifying the version of an R-IN32M3. When read, 0000 0002H is returned.

Remark In the old products, the value read from this register is 0000 0001H.
For details of the old products, see section 1.1, Type Names of R-IN32M3-Series Products.

* Applicable item except yellow hatched is unified description.

28. 21.6 CPURESET register (CPURESET)
Register symbol added. (p.21-6)

Rev7.00:

21.6 CPURESET register

This register is used to end the reset executed by the host CPU on the Cortex-M3 CPU in the R-IN32M3 when the host is booted.
The initial value after reset ends varies depending on the setting of the BOOT1 and BOOT0 pins. It is only permitted to write 0 to this register (to clear the register).

- Access: This register can be read and written in 32-bit or 16-bit units.

Cautions 1. This register is only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register.
2. Clearing the REMAP register to 0 is ignored.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CPURESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET	BASE +0210H
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W

Note

Bit Position	Bit Name	Description
31 to 1	-	Reserved. When writing to these bits, write 0. When read, 0 is returned.
0	RESET	End the reset of the Cortex-M3 CPU in the R-IN32M3. 0: The CPU is being reset. 1: End the CPU reset.

Note: The initial value changes with the state of the BOOT1 and BOOT0 pins.

BOOT1, BOOT0	Initial value
00	1
01	1
10	0
11	1

Rev8.00:

21.6 CPURESET register (CPURESET)

This register is used to release the Cortex-M3 CPU of an R-IN32M3 from the reset state by the host CPU when the host is booted.
The initial value after release from the reset state depends on the settings for the BOOT1 and BOOT0 pins. This register can be used to release the CPU from the reset state, but it cannot be used to reset the CPU again.

- Access: This register can be read and written in 32- or 16-bit units.

Cautions 1. This register is only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register.
2. Clearing the REMAP register to 0 is ignored.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CPURESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET	BASE +0210H
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W

Note

Bit Position	Bit Name	Description
31 to 1	-	Reserved. When writing to these bits, write 0. When read, 0 is returned.
0	RESET	Releases the Cortex-M3 CPU of an R-IN32M3 from the reset state. 0: The CPU is reset. 1: Releases the CPU from the reset state.

Note: The initial value changes with the state of the BOOT1 and BOOT0 pins.

BOOT1, BOOT0	Initial value
00	1
01	1
10	0
11	1

29. 21.12 CPU Bus Operating Mode Register (CPUBUSMD)

“21.12 CPU Bus Operating Mode Register (CPUBUSMD)”, added. (p.21-31)

Rev7.00:

No descriptions.

Rev8.00:

21.12 CPU Bus Operating Mode Register (CPUBUSMD)

This register is for switching the operating mode of the CPU buses between single transfer and undefined-length burst transfer.
For how to use this register, see section 4.1, Bus Occupancy by the Cortex-M3.

- Access This register can be read and written in 32- or 16-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CPUBUSMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BUSMD	BASE +0214H
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0001H	0000
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	

Bit Position	Bit Name	Description
31 to 1	–	Reserved. When writing to these bits, write 0. When read, 0 is returned.
0	BUSMD	Selects the transfer mode of the Cortex-M3 CPU system bus and Cortex-M3 CPU D code bus. 0: Single transfer 1: Undefined-length burst transfer

Remark The old products do not support this register.
For the old products, see section 1.1, Type Names of R-IN32M3-Series Products.