Date: Mar. 24, 2017

# RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

| Product Category | System LSI | Document No. | TN-RIN-A021A/E | Rev. | 1.00 |
|---|---|---|---|---|---|
| Title | Notification of R-IN32M3 Series User's Manual: Board design edition (Rev. 2.04 to Rev. 3.00)<br>Revised contents: Corrections and new functions | | Information Category | Technical Notification | |
| Applicable Product | See following | Lot No.<br>All lots | Reference Document | R-IN32M3 Series User's Manual: Board design edition<br>R-IN32M3-EC<br>R-IN32M3-CL<br>Rev.3.00<br>(R18UZ0021EJ0300) | |

R-IN32M3 Series User's Manual: Board design edition (for R-IN32M3-EC and R-IN32M3-CL) Rev. 3.00 (R18UZ0021EJ0300) has been released on Renesas website. For details, see "2. Documentation Updates" below.

## 1 Applicable Product

| Product Type | Model Marking | Product Code |
|---|---|---|
| R-IN32M3-EC | MC-10287F1 | MC-10287F1-HN4-A |
| | | MC-10287F1-HN4-M1-A |
| | MC-10287BF1 | MC-10287BF1-HN4-A |
| | | MC-10287BF1-HN4-M1-A |
| R-IN32M3-CL | D60510F1 | UPD60510F1-HN4-A |
| | | UPD60510F1-HN4-M1-A |
| | D60510BF1 | UPD60510BF1-HN4-A |
| | | UPD60510BF1-HN4-M1-A |

## 2 Documentation Updates

(1/2)

| No. | Applicable Item (Rev. 3.00 Section) | Applicable Page (Rev. 3.00) | Contents |
|---|---|---|---|
| 1 | 1.1 Definition of Pin Handling and Symbols in This Manual | 1 | Complement |
| 2 | 3.3 Oscillation Circuit Configuration Example | 8 | Expression alignment |
| 3 | 3.3 Oscillation Circuit Configuration Example | 8 | Complement |
| 4 | 4.1 Recommended Configuration of Filter | 9 | Expression alignment |
| 5 | 5.1 Built-in Regulator Used | 11 | Complement |
| 6 | 5.1 Built-in Regulator Used | 12 | Complement |
| 7 | 5.2 Built-in Regulator Unused | 13 | Complement |
| 8 | 6. GPIO Port Pins | 14 | Errors corrected |
| 9 | 7. Ethernet PHY Pins (R-IN32M3-EC Only) | 15 | Complement |
| 10 | 7.1 Ethernet PHY Power Supply Pins | 15 | Errors corrected |
| 11 | 7.2 100Base-TX Pins | 16 | Complement |
| 12 | 7.2 100Base-TX Pins | 17 | Errors corrected |
| 13 | 7.2 100Base-TX Pins | 17 | Complement |
| 14 | 7.3 100Base-FX Pins (Optical Fiber) | 20 | Errors corrected |
| 15 | 8. GMII Pins (R-IN32M3-CL Only) | 21 | Expression alignment |
| 16 | 8.2 Circuit Design around GMII | 22 | Errors corrected |
| 17 | 9. CC-Link Pins | 24 | Errors corrected |
| 18 | 11. External MCU/Memory Interface Pins | 26 | Complement |
| 19 | 11.1.1 Asynchronous SRAM Interface Mode | 28 | Expression alignment |
| 20 | 11.1.2 Synchronous SRAM Interface Mode | 30 | Expression alignment |
| 21 | 11.1.3 Synchronous SRAM-Type Transfer Mode | 32 | Expression alignment |
| 22 | 11.2 External Memory Interface | 34 | Expression alignment |
| 23 | 11.2.1.1 Connection Example with SRAM | 35 | Expression alignment |
| 24 | 11.2.2.1 Connection Example with SRAM | 38 | Expression alignment |
| 25 | 11.2.2.2 Connection Example with Paged ROM | 39 | Expression alignment |
| 26 | 12. Serial Flash ROM Connection Pins | 37 | Complement |
| 27 | 13. Asynchronous Serial Interface J Connection Pins | 38 | Complement |
| 28 | 14. $I^2C$ Connection Pins | 39 | Complement |
| 29 | 15. EtherCAT EEPROM $I^2C$ Connection Pins (R-IN32M3-EC Only) | 40 | Complement |
| 30 | 16. CAN Pins | 41 | Complement |
| 31 | 17. JTAG/Trace Pins | 42 | Complement |

(2/2)

| No | Applicable Item (Rev. 9.01 Section) | Applicable Page (Rev. 9.01) | Contents |
|---|---|---|---|
| 32 | 17. JTAG/Trace Pins | 43 | Complement |
| 33 | 17. JTAG/Trace Pins | 44 | Complement |
| 34 | 22. IBIS Information | 51 | Errors corrected |
| 35 | 23.1 R-IN32M3-EC | 52 | Errors corrected |
| 36 | 23.2 R-IN32M3-CL | 52 | Errors corrected |
| 37 | 24. Guide to Thermal Design | 53 to 61 | Complement |

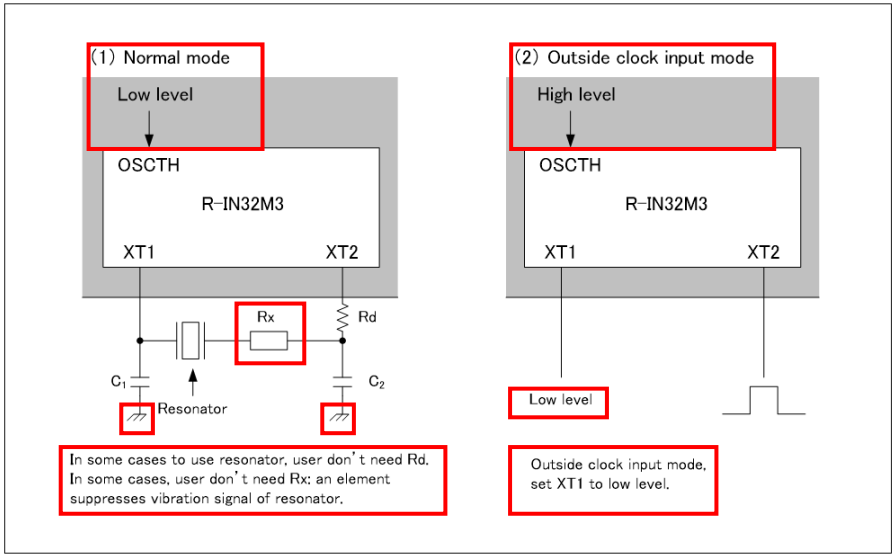
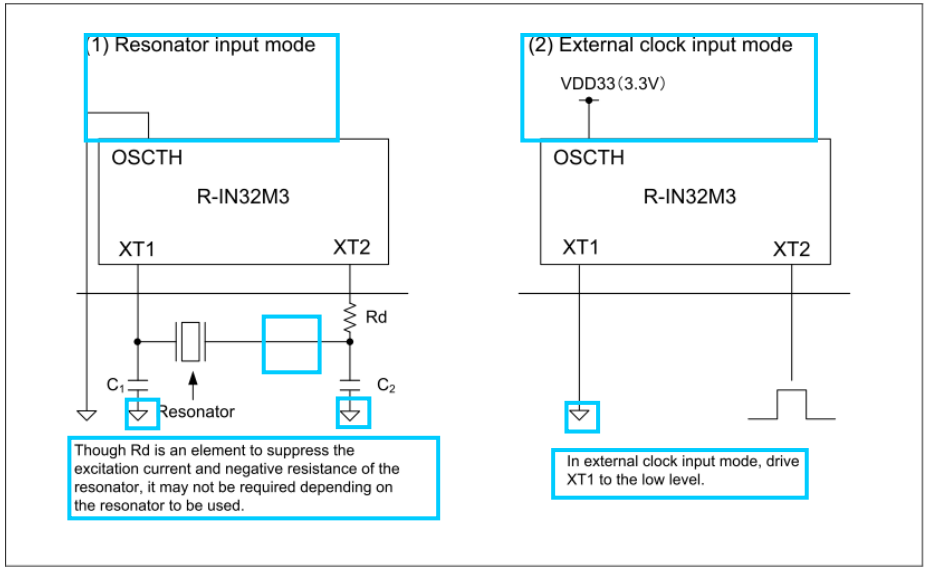
## No.1 1.1 Definition of Pin Handling and Symbols in This Manual

**"1.1 Definition of Pin Handling and Symbols in This Manual" was newly added.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 1 | (Not described) | 1 | **[1.1 Definition of Pin Handling and Symbols in This Manual]** |

## No.2 3.3 Oscillation Circuit Configuration Example

**Pin handling and the GND description in Figure 3.2 were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 7 | **[3.3 Oscillation circuit configuration example]**<br>  <br><br>Figure 3.2 Configuration example of the oscillation circuit | 7 | **[3.3 Oscillation Circuit Configuration Example]**<br>  <br><br>Figure 3.2 Configuration Example of the Oscillation Circuit |

## No.3 3.3 Oscillation Circuit Configuration Example

**Caution on a resonator was modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 7 | **[3.3 Oscillation circuit configuration example]**<br>[Figure 3.2 Configuration example of the oscillation circuit]<br><br>Caution R-IN32M3's input is fixed 25MHz. Load of resonator should be 8pF or lower.<br>But it depends on the resonator and the design situation. Please consult the design information given by the resonator manufacturer | 7 | **[3.3 Oscillation Circuit Configuration Example]**<br>[Figure 3.2 Configuration Example of the Oscillation Circuit]<br><br>Caution. The input of the R-IN32M3 is fixed to 25 MHz.<br>When a resonator is to be used, contact the resonator manufacturer and ask for a corresponding part number and external constants.<br>Renesas recommends the following oscillator and resonator manufacturers.<br><br>• Nihon Dempa Kogyo Co., Ltd. (NDK)<br>URL: http://www.ndk.com/jp/index.html/<br>• KYOCERA Crystal Device Corporation<br>URL: http://www.kyocera-crystal.jp/ |

## No.4 4.1 Recommended Configuration of Filter

**Pin handling and the GND description in Figure 4.1 were modified.**

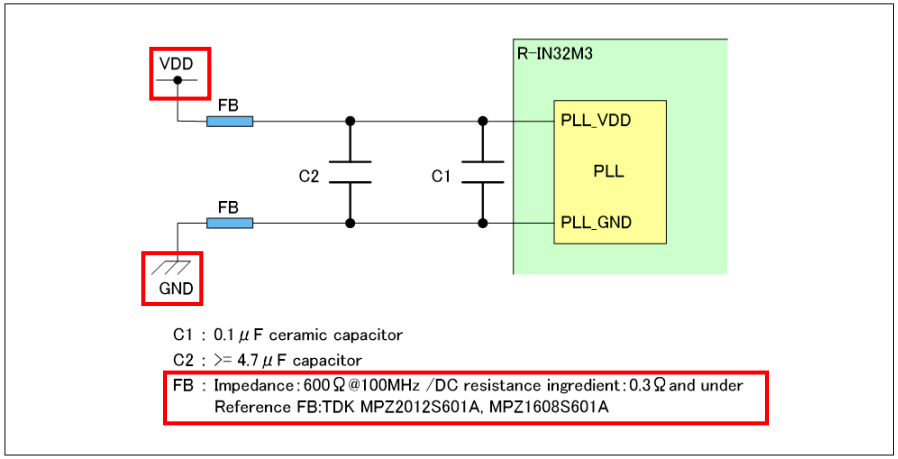
<table>
<tr><th colspan="2">V2.04</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description Contents</th><th>Page</th><th>Revised Contents</th></tr>
<tr><td>8</td><td>[4.1 Recommended FILTER composition]<br> 

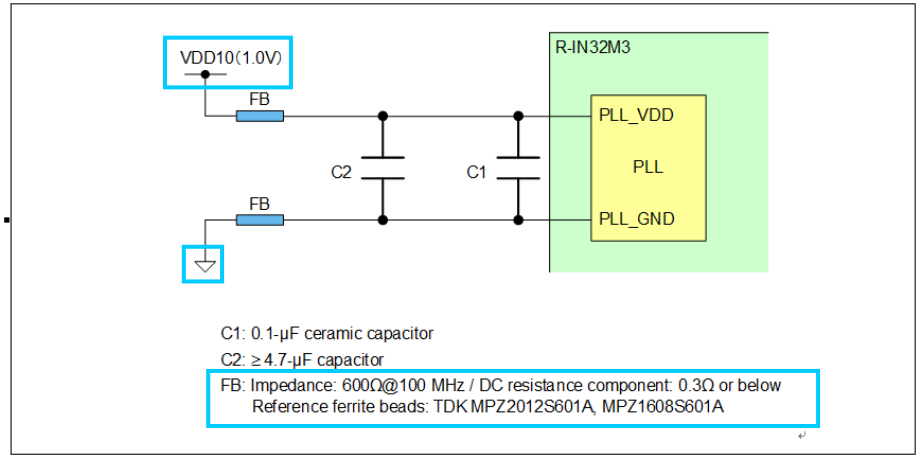
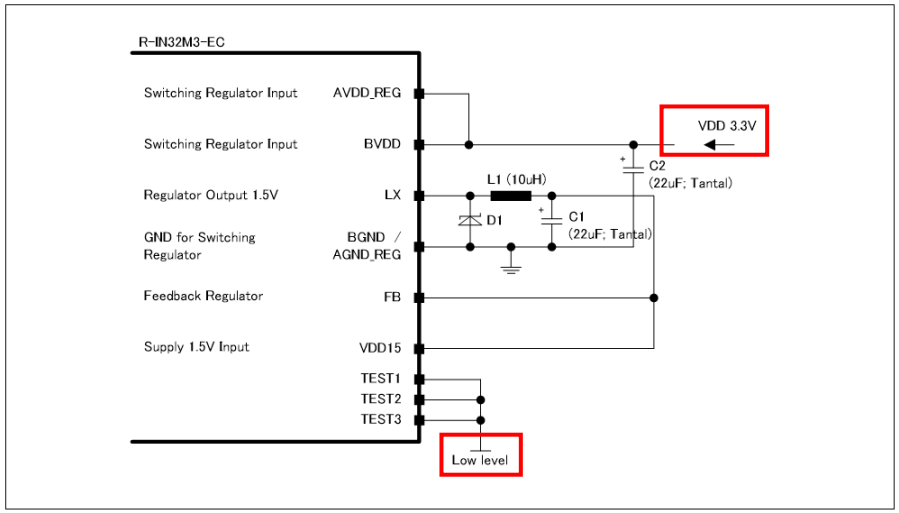
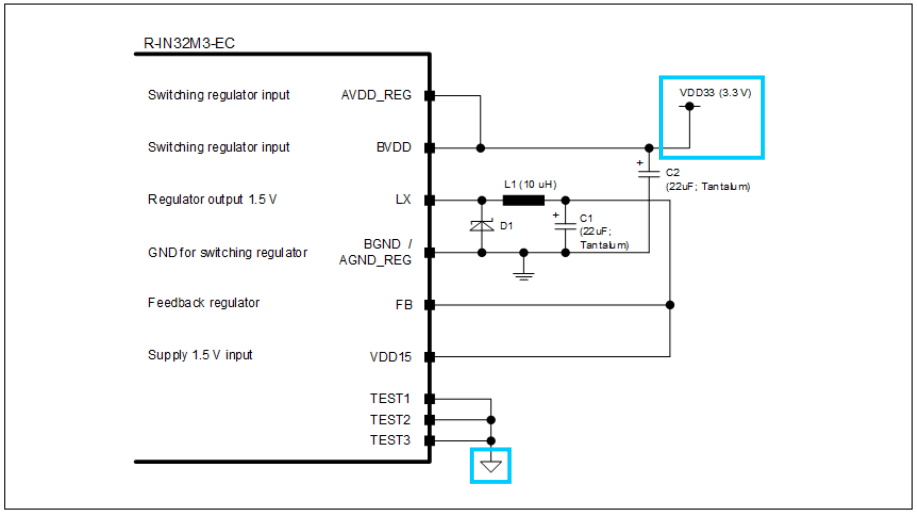
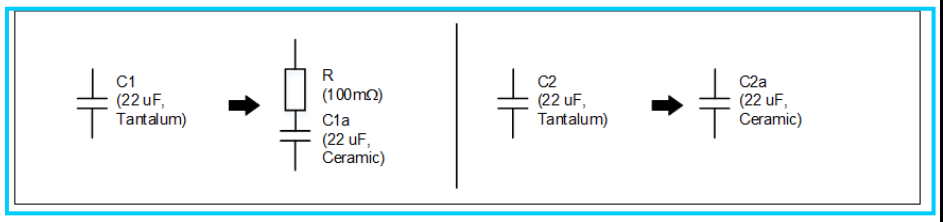
Figure 4.1 Recommended FILTER composition</td><td>8</td><td>[4.1 Recommended Configuration of Filter]<br> 

Figure 4.1 Recommended Configuration of Filter</td></tr>
</table>

## No.5 5.1 Built-in Regulator Used

**Pin handling and the GND description in Figure 5.1 were modified. The description on the capacitor substitution method was added.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 10 | **[5.1 Built-in regulator used]**<br>  <br><br>Figure 5.1 Wiring example of the regurator unit (internal regulator used) | 10 | **[5.1 Built-in Regulator Used]**<br>  <br><br>Figure 5.1 Wiring Example of the Regulator Unit (Built-in Regulator Used)<br><br>If tantalum capacitors are not available, it is possible to use a resistor and a ceramic capacitor for C1, and a ceramic capacitor for C2.<br>  <br> |

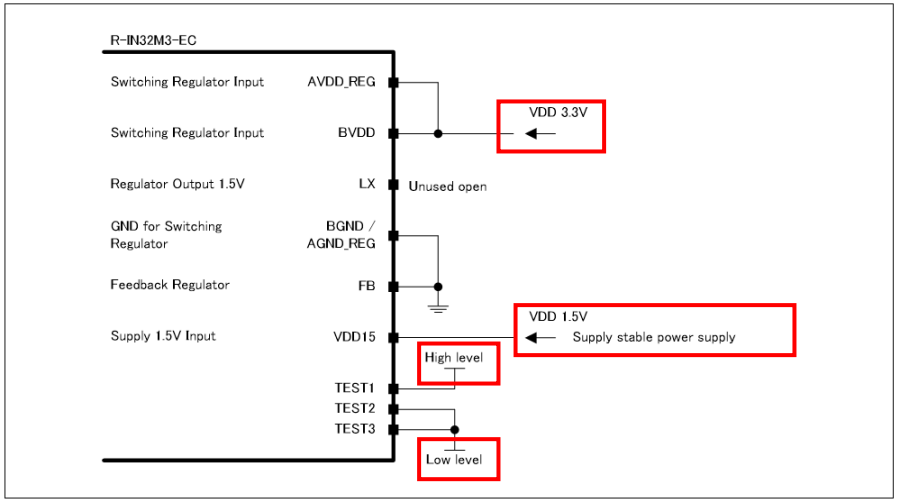
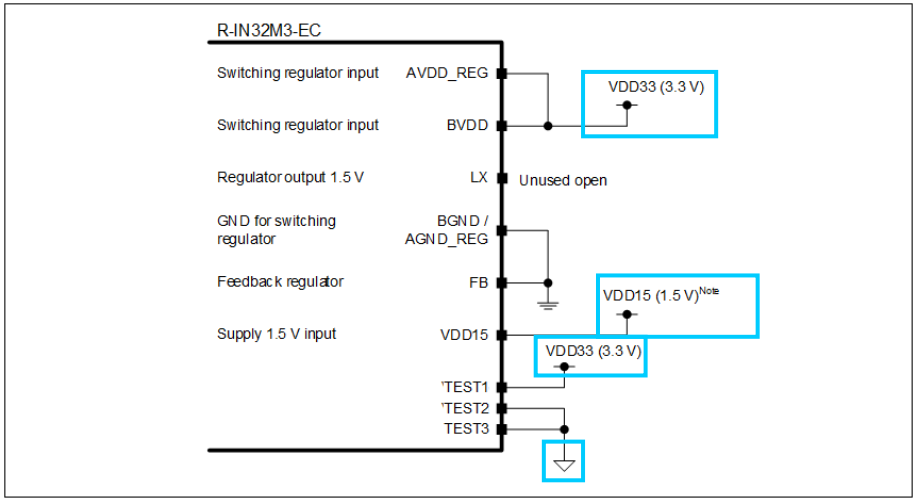
## No.6 5.1 Built-in Regulator Used

**Table 5.1 was added to complement the list of the recommended parts.**

<table>
<tr><th colspan="2">V2.04</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description Contents</th><th>Page</th><th>Revised Contents</th></tr>
<tr><td>11</td><td>[5.1 Built-in regulator used]<br>Use recommended parts<br>・D1 : Schottky diode (STPS1L30UPBF, Vishay)<br>・L1 : Inductor 10μH (VLCF5028T provided by TDK)<br>・C1, C2 : Capacitor 22μF Tantal (ESR = 300mΩ), PSLB21A226M, NEC Tokin</td><td>11</td><td>[5.1 Built-in Regulator Used]<br>[Table 5.1 List of Recommended Parts for Use]
<table>
<tr><th>Parts</th><th>Type</th><th>Characteristics</th><th>Recommend Ports</th></tr>
<tr><td>D1</td><td>Schottky diode</td><td>30 V, 1 A</td><td>STPS1L30UPBF (ST)</td></tr>
<tr><td>L1</td><td>Inductor</td><td>10 uH</td><td>VLC5028T (TDK)</td></tr>
<tr><td>C1, C2</td><td>Tantalum capacitor</td><td>22 uF±20%<br>ESR: 75 to 300 mΩ</td><td>PSLB21A226M (NEC TOKIN)</td></tr>
<tr><td>C1a, C2a</td><td>Ceramic capacitor</td><td>22 uF±10%</td><td>GRM32ER71A226KE20L (Murata)</td></tr>
<tr><td>R</td><td>Resistor</td><td>100 mΩ±1%</td><td>MCR18EZHFLR100 (ROHM)</td></tr>
</table></td></tr>
</table>

## No.7 5.2 Built-in Regulator Unused

**Pin handling and the GND description in Figure 5.3 were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 12 | **[5.2 Built-in regulator unused]**<br>  <br>Figure 5.3 Wiring example of the regulator unit (internal regulator is not used) | 12 | **[5.2 Built-in Regulator Unused]**<br>  <br>Figure 5.3 Wiring Example of the Regulator Unit (Internal Regulator is Not Used)<br>**Note. Supply stable power supply.** |

## No.8 6. GPIO Port Pins

**The reference in separate user's manuals, modified**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 13 | **[6. GPIO port pins]**<br>GPIO is general purpose IO port. Regarding internal structure, please refer below document.<br>R-IN32M3-EC: User's Manual R-IN32M3-EC 2.3.5 Port Signals<br>R-IN32M3-CL: User's Manual R-IN32M3-CL 2.5.5 Port Signals | 13 | **[6. GPIO Port Pins]**<br>GPIO is a general-purpose I/O port. As for the internal configuration, see the section in the following document.<br>R-IN32M3-EC: User's Manual R-IN32M3-EC "2.3.6 Port Signals"<br>R-IN32M3-CL: User's Manual R-IN32M3-CL "2.5.6 Port Signals" |

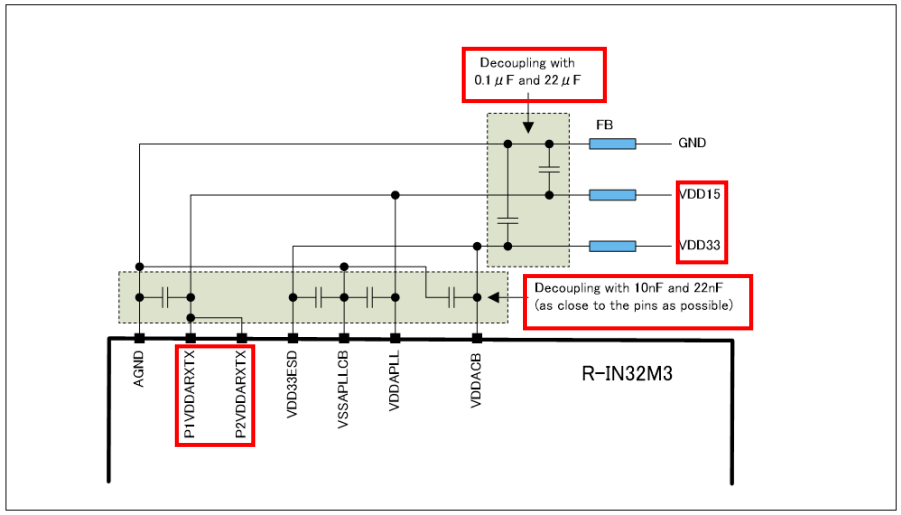
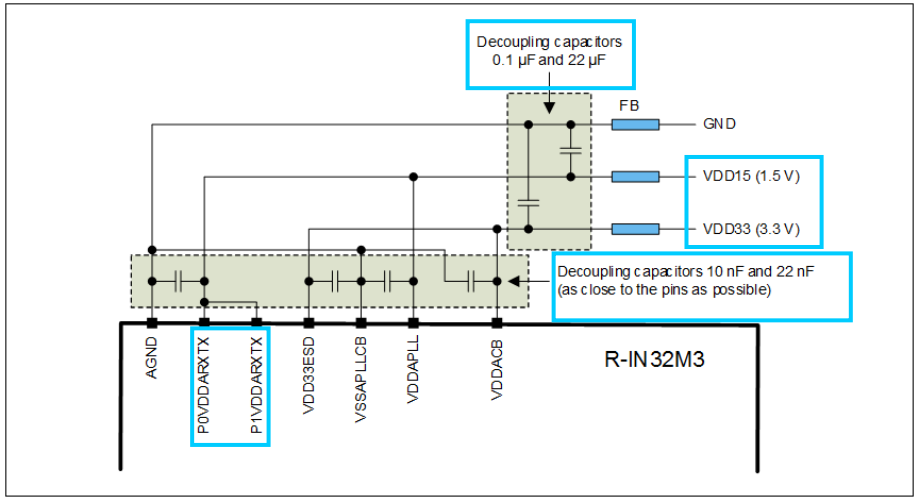
## No.9 7. Ethernet PHY Pins (R-IN32M3-EC Only)

**The description that this section was for the R-IN32M3-EC only was added to the section title.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 14 | **[7. Ethernet PHY pins]** | 15 | **[7. Ethernet PHY Pins (R-IN32M3-EC Only)]** |

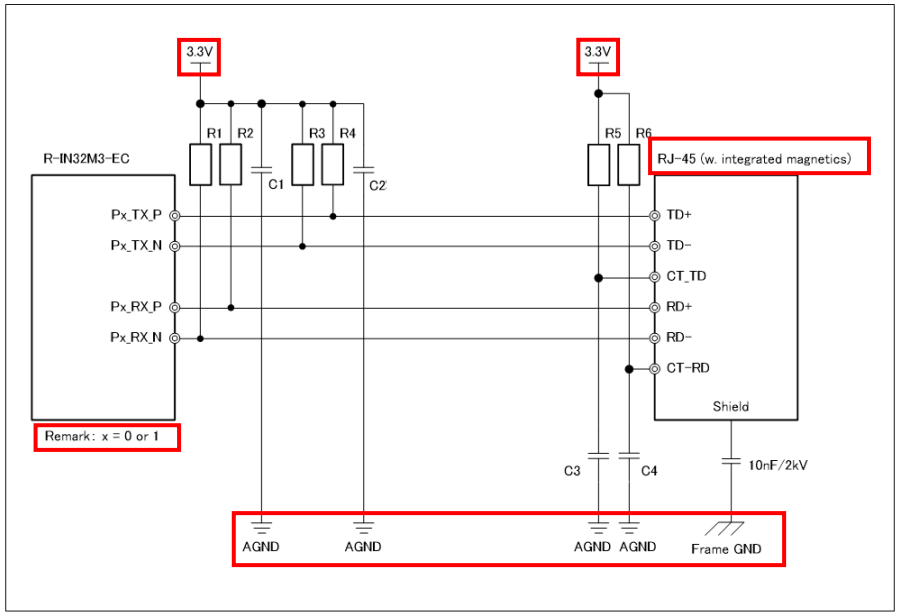
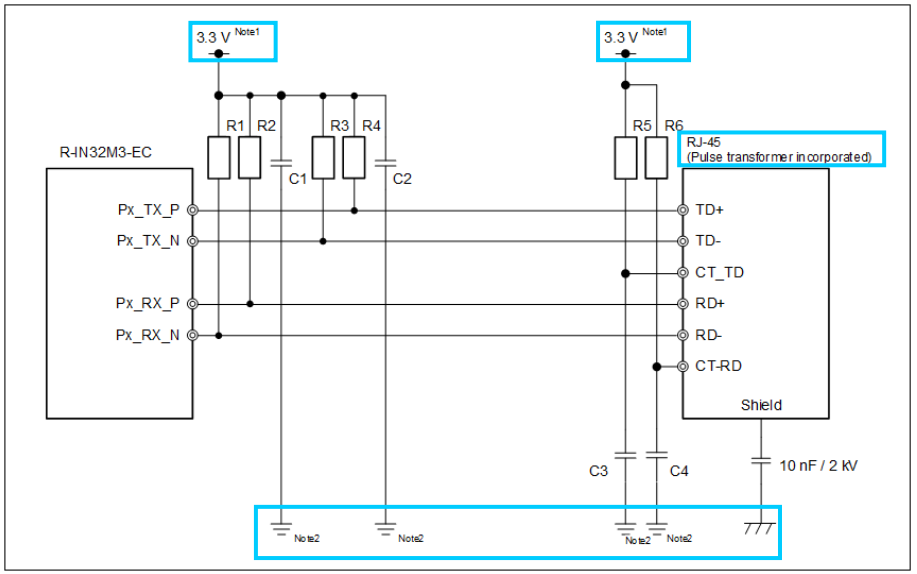
## No.10 7.1 Ethernet PHY Power Supply Pins

**Pin names of Rx/Tx analog power supply pins and the description of power supply pins were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 14 | **[7.1 Ethernet PHY power supply pins]**<br>  <br><br>Figure 7.1 Wiring example of the regulator unit | 14 | **[7.1 Ethernet PHY Power Supply Pins]**<br>  <br><br>Figure 7.1 Decoupling Capacitors for Power Supply |

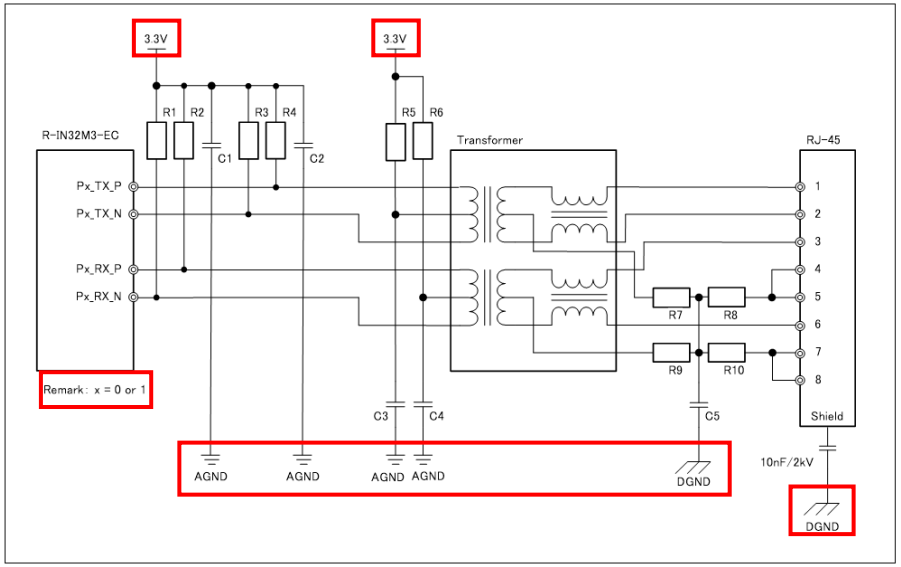
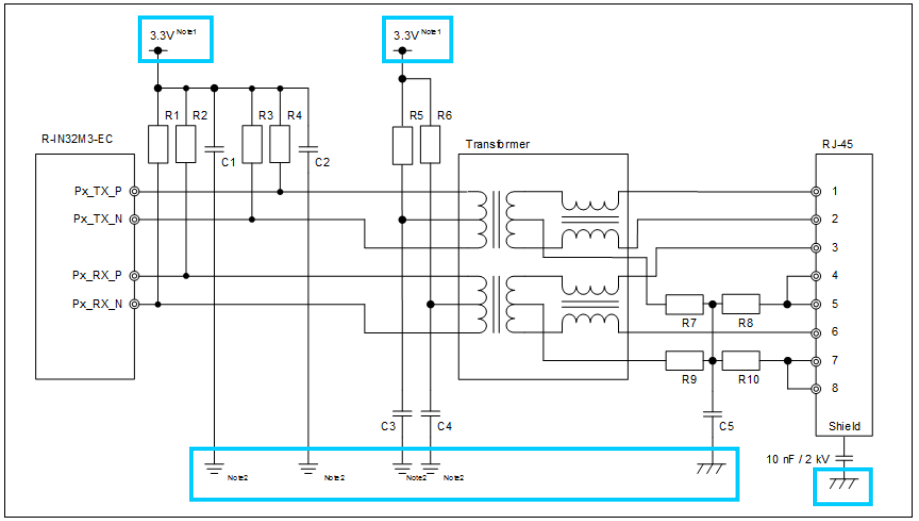
## No.11 7.2 100Base-TX Pins

**Pin handling and the GND description in Figure 7.2 were modified. Remark and Notes were moved to outside of the figure frame.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 15 | **[7.2 100Base -TX pins]**<br>  <br><br>Figure 7.2 Connection example R-IN32M3-EC and RJ-45 connector(pulse transformer built-in) | 15 | **[7.2 100Base-TX Pins]**<br>  <br><br>Figure 7.2 Connection Example of R-IN32M3-EC and RJ-45 Connector (Pulse Transformer Incorporated)<br>**Remark. x = 0 or 1**<br>**Notes 1. Same potential with VDDACB and VDD33ESD**<br>**2. Same potential with AGND** |

## No.12 7.2 100Base-TX Pins

**Pin handling and the GND description in Figure 7.3 were modified. Remark and Notes were moved to outside of the figure frame.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 16 | **[7.2 100Base -TX pins]**<br>  <br><br>Figure 7.3 Connection example R-IN32M3-EC and Pulse transformer and RJ-45 connector | 16 | **[7.2 100Base-TX Pins]**<br>  <br><br>Figure 7.3 Connection Example of R-IN32M3-EC, Pulse Transformer, and RJ-45 Connector<br>**Remark. x = 0 or 1**<br>**Notes 1. Same potential with VDDACB and VDD33ESD**<br>**2. Same potential with AGND** |

## No.13 7.2 100Base-TX Pins

**Note was added to R1 to R6 in Table 7.1.**

### V2.04

| Page | Description Contents |
|---|---|
| 16 | **[7.2 100Base -TX pins]**<br>[Table 7.1 Parts list (100Base-TX interface)] |

| Part | Type | Characteristics | Recommended components |
|---|---|---|---|
| R1, R2, R3, R4 | Resistor | 49.9Ω ±1% 1/16W | – |
| R5, R6 | Resistor | 10Ω ±1% 1/16W | – |
| R7, R8, R9, R10 | Resistor | 75Ω ±1% 1/16W | – |
| C1 | Capacitor | 10nF - 100nF | – |
| C2 | Capacitor | 10nF - 100nF | – |
| C3 | Capacitor | 10nF - 22nF | – |
| C4 | Capacitor | 10nF - 22nF | – |
| C5 | Capacitor | 4.7nF ±10% | – |
| Transformer | | One channel | Pulse Electronics H1012NL, H1102NL |
| | | Twochannel | Pulse Electronics H1270N+, HX1294 |
| RJ45 with integrated magnetics | | Two channel | Pulse Electronics JG0-0031NL |

### V3.00

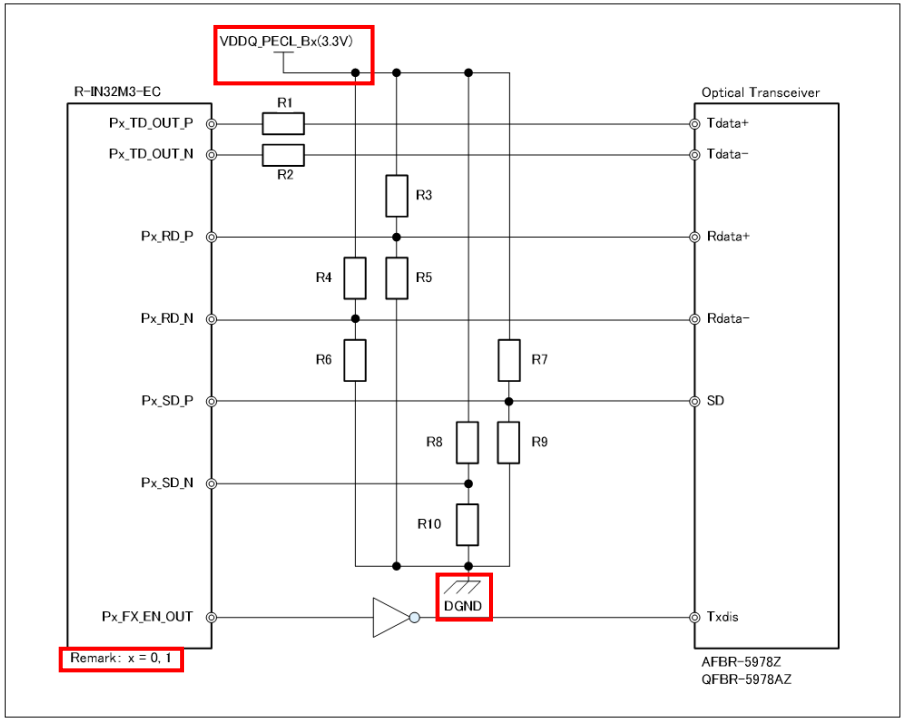
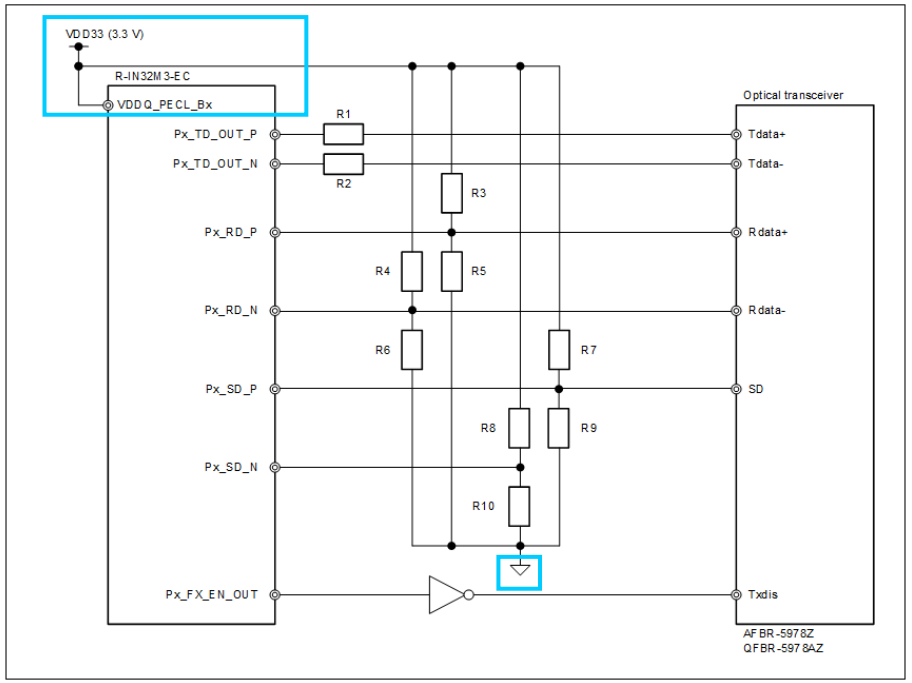
| Page | Revised Contents |
|---|---|
| 16 | **[7.2 100Base-TX Pins]**<br>[Table 7.1 Parts List (100Base-TX interface)] |

| Part | Type | Characteristics | Recommended Components |
|---|---|---|---|
| R1, R2, R3, R4 | Resistor | 49.9Ω±1% 1/16W Note | - |
| R5, R6 | Resistor | 10Ω±1% 1/16W Note | - |
| R7, R8, R9, R10 | Resistor | 75Ω±1% 1/16W | - |
| C1 | Capacitor | 10 nF to 100 nF | - |
| C2 | Capacitor | 10 nF to 100 nF | - |
| C3 | Capacitor | 10 nF to 2 2 nF | - |
| C4 | Capacitor | 10 nF to 22 nF | - |
| C5 | Capacitor | 4.7 nF±10% | - |
| Pulse transformer | | One channel | Pulse Electronics H1012NL, H1102NL |
| | | Two channels | Pulse Electronics H1270N+, HX1294 |
| RJ-45 connector (Pulse transformer incorporated) | | Two channels | Pulse Electronics JG0-0031NL |

**Note. We recommend 1/8W when using in harsh environments, such as at high temperature.**

## No.14 7.3 100Base-FX Pins (Optical Fiber)

**Pin handling and the GND description in Figure 7.7 were modified. Remark was moved to outside of the figure frame.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 19 | **[7.3 100Base-FX pins (Optical fiber)]**<br>  <br><br>Figure 7.7 Interface circuit with optical transceiver | 19 | **[7.3 100Base-FX Pins (Optical Fiber)]**<br>  <br><br>Figure 7.7 Interface Circuit with Optical Transceiver<br>**Remark. x = 0 or 1** |

## No.15 8. GMII Pins (R-IN32M3-CL Only)

**Pin handling in Figure 8.1 was modified. Remark was moved to outside of the figure frame.**

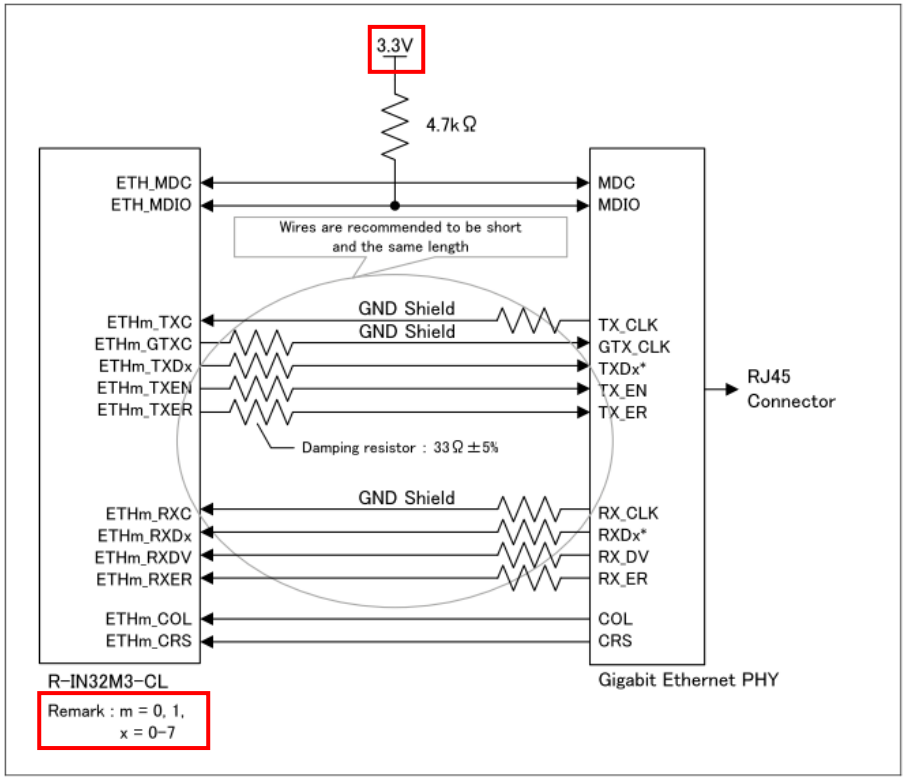
<table>
<tr><th colspan="2">V2.04</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description Contents</th><th>Page</th><th>Revised Contents</th></tr>
<tr><td>20</td><td>[8. GMII pins (R-IN32M3-CL only)]<br> 

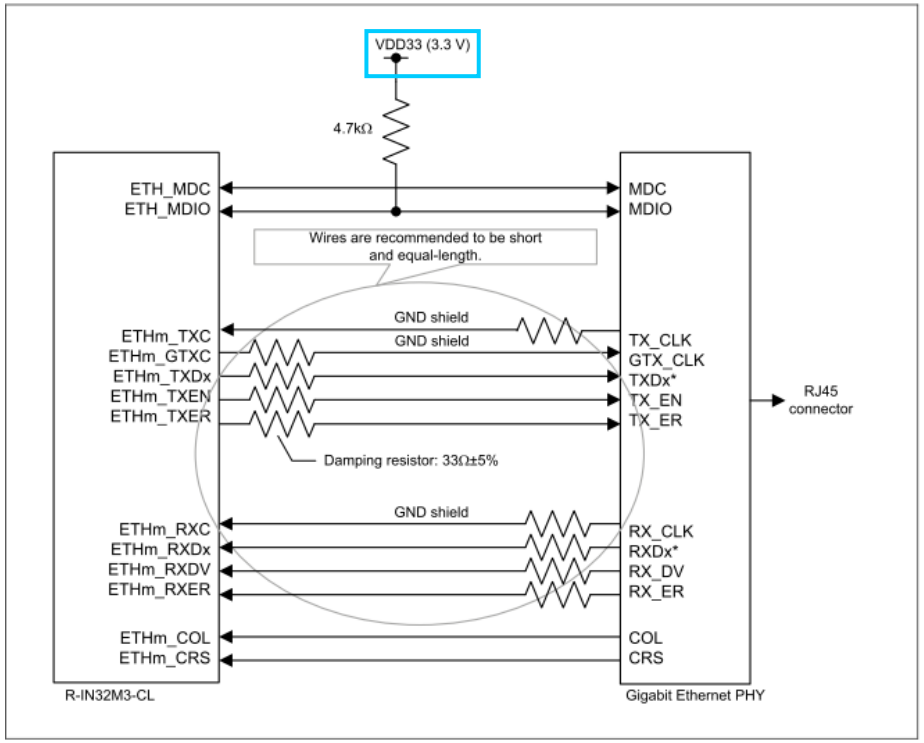
Figure 8.1 Connection image of R-IN32M3-CL and PHY</td><td>20</td><td>[8. GMII Pins (R-IN32M3-CL Only)]<br> 

Figure 8.1 Connection Image of R-IN32M3-CL and Gigabit Ethernet PHY<br><br>Remark. m = 0, 1, x = 0 to 7</td></tr>
</table>

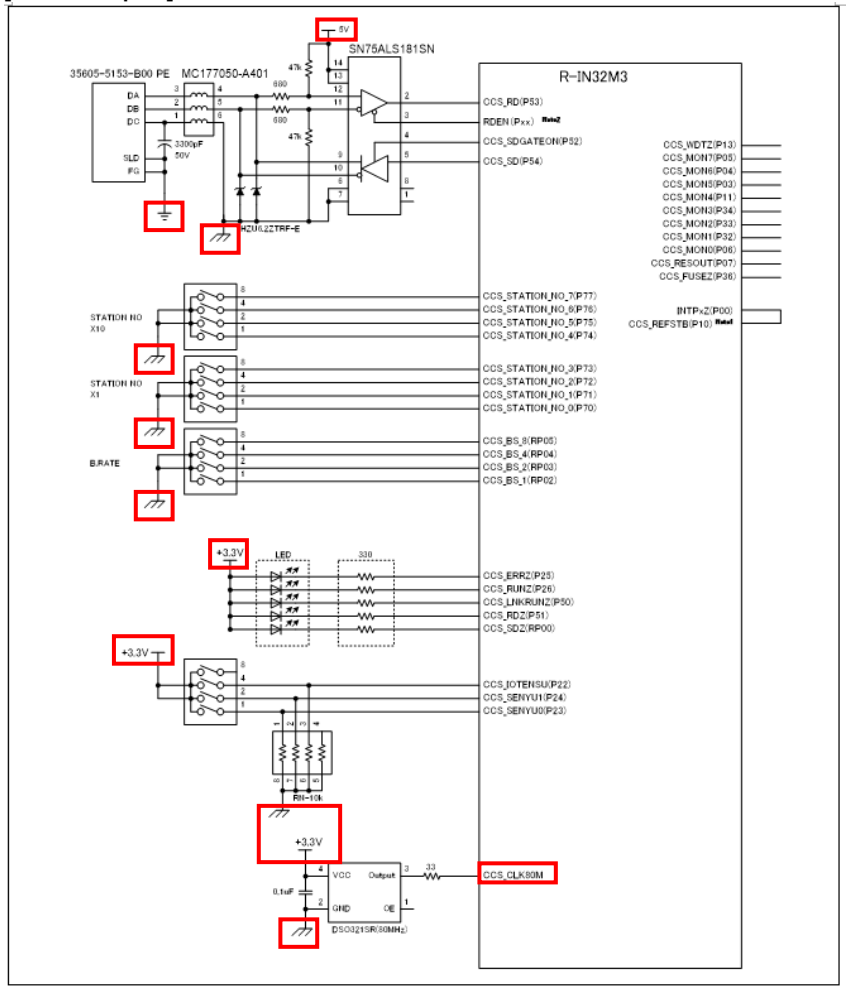
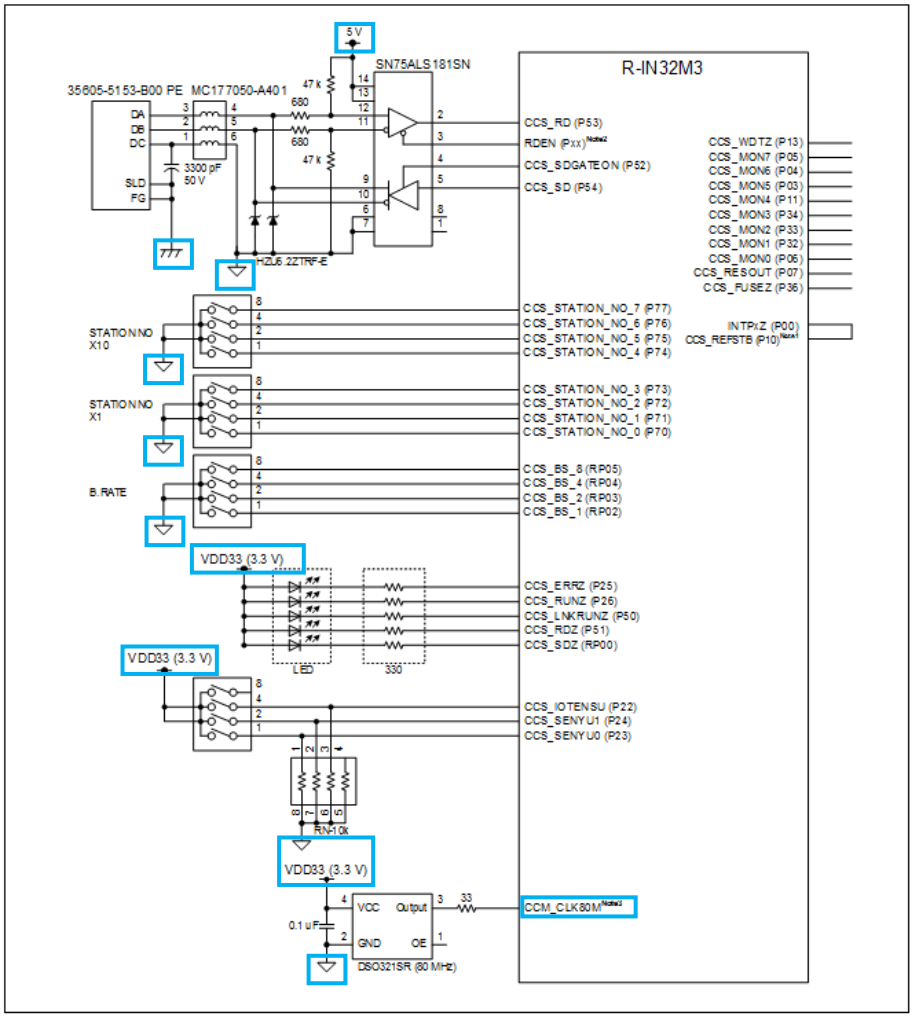
## No.16 8.2 Circuit Design around GMII

**The description of the number for Ethernet ports was modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 21 | **[8.2 Circuit design around GMII]**<br><br>Please be set to the same address as the port mumber of the R-IN32M3-CL and The PHY address.<br>Connect to the PHY assigned address1 to MAC port1, And Connect to the PHY assigned address2 to MAC port2 | 21 | **[8.2 Circuit Design around GMII]**<br><br>• For PHY address<br>Set to the same address as the port number of the R-IN32M3-CL to the PHY address.<br>Connect the PHY assigned to address 0 to MAC port 0, and connect the PHY assigned to address 1 to MAC port 1. |

## No.17 9. CC-Link Pins

**Pin handling and the GND description in Figure 9.1 were modified. The name for CC-Link clock pins was modified. Note 3 was added.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 23 | **[9. CC-Link pins]**<br>  <br><br>Figure 9.1 The connection example for CC-Link Remote device station<br>**Note1**<br>**Note2** | 23 | **[9. CC-Link Pins]**<br>  <br><br>Figure 9.1 Connection Example for CC-Link Remote Device Station<br>**Notes 1.**<br>**2.**<br>**3. This pin is multiplexed with CC-Link (intelligent device station).** |

## No.18 11. External MCU/Memory Interface Pins

**As the mode setting pin, the ADMUXMODE pin was added. Note when accessing the CC-Link IE field wad added.**

<table>
<tr><th colspan="2">V2.04</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description Contents</th><th>Page</th><th>Revised Contents</th></tr>
<tr><td>25</td><td>

**[11. External MPU/memory interface pins]**

The connection mode is decided as Table 11.1 by the signal level of the MEMIFSEL pin, MEMCSEL pin and HIFSYNC pin.

Table 11.1 The mode selecton of external MPU/memory connection

<table>
<tr><th colspan="3">Mode setting</th><th rowspan="2">The connection mode to external parts</th></tr>
<tr><th>MEMIFSEL</th><th>MEMCSEL</th><th>HIFSYNC</th></tr>
<tr><td rowspan="5">Low</td><td rowspan="2">Low</td><td>-</td><td>External memory interface<br>Asynchronous SRAM MEMC</td></tr>
<tr><td>High</td><td>-</td><td>External memory interface<br>Synchronous SRAM MEMC</td></tr>
<tr><td rowspan="3">High</td><td rowspan="2">Low</td><td>Low</td><td>External MPU interface<br>Asynchronous SRAM interface</td></tr>
<tr><td>High</td><td>External MPU interface<br>Synchronous SRAM interface</td></tr>
<tr><td rowspan="2">High</td><td>Low</td><td>Prohibition of a setup</td></tr>
<tr><td>High</td><td>External MPU interface<br>Synchronous SRAM type transmission mode</td></tr>
</table>

</td><td>25</td><td>

**[11. External MCU/Memory Interface Pins]**

The connection mode is decided by the signal level of the MEMIFSEL, MEMCSEL, HIFSYNC, and ADMUXMODE pins as shown in Table 11.1.

Table 11.1 Mode Selection of External MCU/Memory Connection

<table>
<tr><th colspan="4">Mode Setting</th><th rowspan="2">External Connection Mode</th></tr>
<tr><th>MEMIFSEL</th><th>MEMCSEL</th><th>HIFSYNC</th><th>ADMUXMODE</th></tr>
<tr><td rowspan="2">Low</td><td>Low</td><td>-</td><td>-</td><td>External memory interface<br>Asynchronous SRAM MEMC</td></tr>
<tr><td>High</td><td>-</td><td>-</td><td>External memory interface<br>Synchronous burst access MEMC</td></tr>
<tr><td rowspan="4">High</td><td rowspan="2">Low</td><td>Low</td><td>-</td><td>External MCU interface<br>Asynchronous SRAM interface mode</td></tr>
<tr><td>High</td><td>-</td><td>External MCU interface<br>Synchronous SRAM interface mode Note</td></tr>
<tr><td rowspan="2">High</td><td>Low</td><td>-</td><td>Setting prohibited</td></tr>
<tr><td>High</td><td>Low</td><td>Setting prohibited</td></tr>
<tr><td colspan="3"></td><td>High</td><td>External MCU interface<br>Synchronous SRAM-type transfer mode<br>(address/data multiplexed)</td></tr>
</table>

Note. Before access to the CC-Link IE field, select the synchronous SRAM interface mode (MEMIFSEL high, MEMCSEL low, HIFSYNC high). (The CC-Link IE field is incorporated only in the R-IN32M3-CL.)

</td></tr>
</table>

## No.19 11.1.1 Asynchronous SRAM Interface Mode

**The description of pin handling in Figure 11.1 and Figure 11.2 was modified. The position for the HBUSCLK pin and Note was modified.**

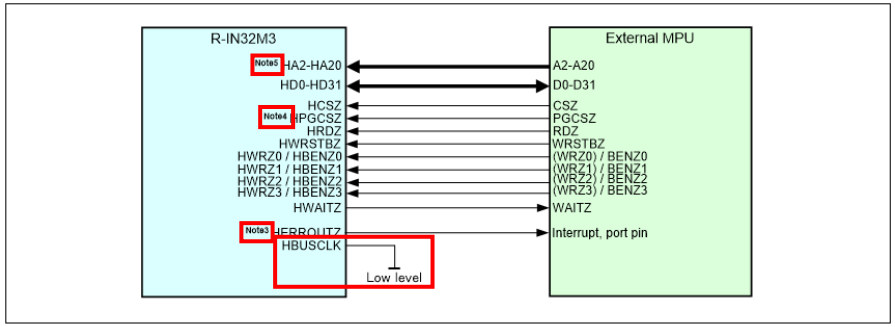
<table>
<tr><th colspan="2">V2.04</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description Contents</th><th>Page</th><th>Revised Contents</th></tr>
<tr><td>26, 27</td><td>[11.1.1 Asynchronous SRAM interface]<br> 

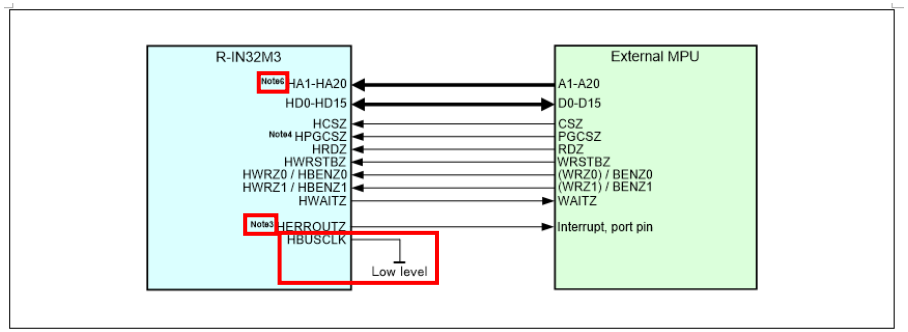
Figure 11.1 The connection example with external MPU (32bit bus, asynchronous SRAM interface mode)<br> 

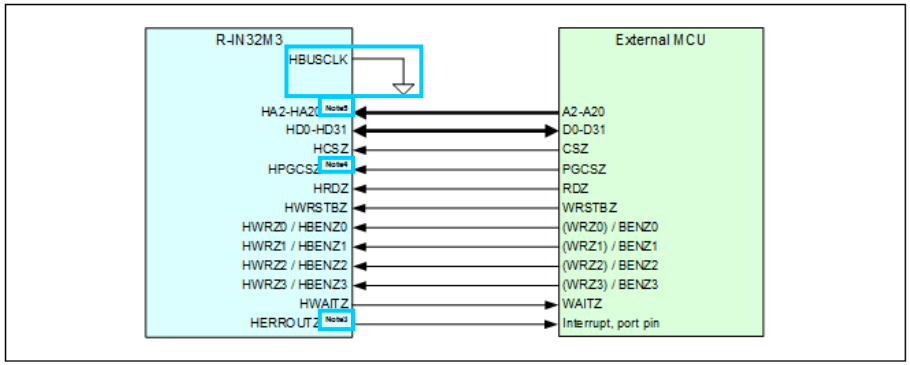
Figure 11.2 The connection example with external MPU (16bit bus, asynchronous SRAM interface mode)</td><td>28</td><td>[11.1.1 Asynchronous SRAM Interface Mode]<br> 

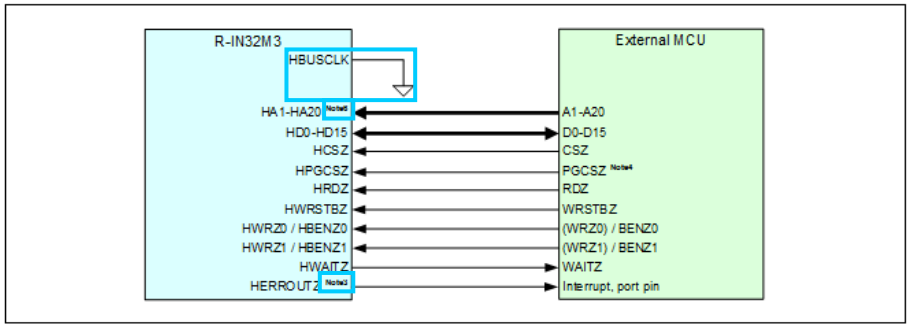
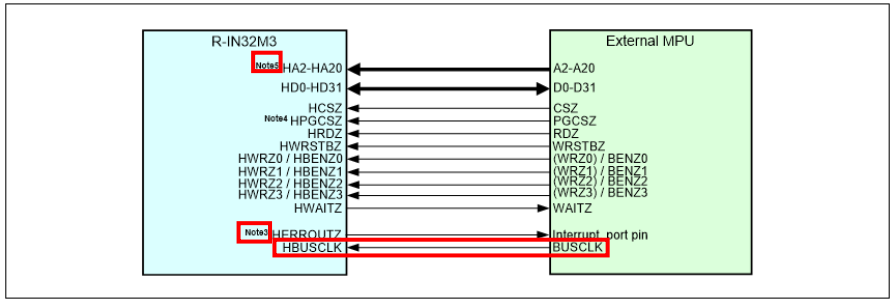
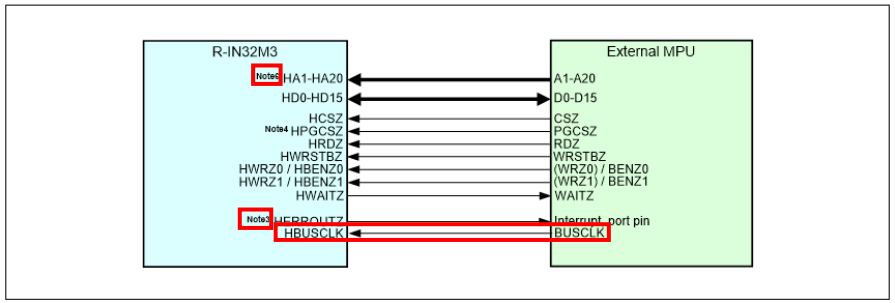
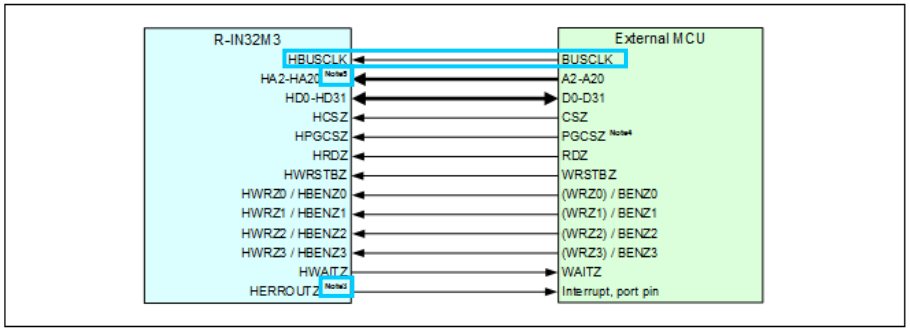
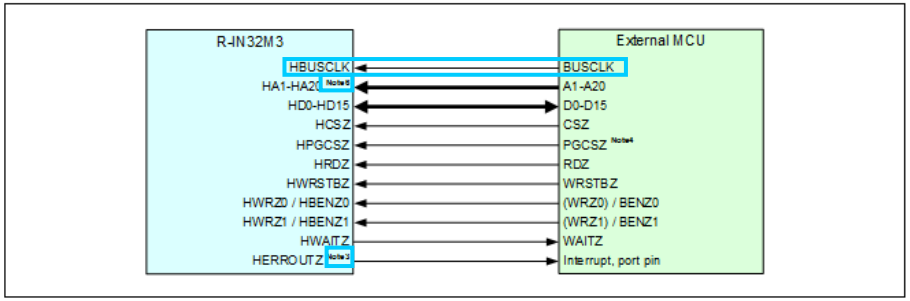
Figure 11.1 Connection Example of 32-Bit External MCU Interface (Asynchronous SRAM Interface Mode)<br> 

Figure 11.2 Connection Example of 16-Bit External MCU Interface (Asynchronous SRAM Interface Mode)</td></tr>
</table>

## No.20 11.1.2 Synchronous SRAM Interface Mode

**The position for the HBUSCLK pin and Note in Figure 11.3 and Figure 11.4 were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 28 | **[11.1.2 Synchronous SRAM interface mode]**<br>  <br><br>Figure 11.3 The connection example with external MPU (32bit bus, synchronous SRAM interface mode)<br>  <br><br>Figure 11.4 The connection example with external MPU (16bit bus, synchronous SRAM interface mode) | 30 | **[11.1.2 Synchronous SRAM Interface Mode]**<br>  <br><br>Figure 11.3 Connection Example of 32-Bit External MCU Interface (Synchronous SRAM Interface Mode)<br>  <br><br>Figure 11.4 Connection Example of 16-Bit External MCU Interface (Synchronous SRAM Interface Mode) |

## No.21 Synchronous SRAM-Type Transfer Mode

**The description of pin handling in Figure 11.5 and Figure 11.6 was modified. The position for the HBUSCLK pin and Note was modified.**

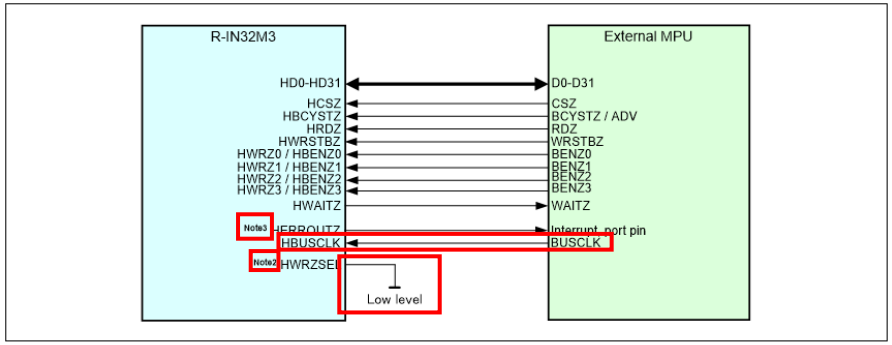
<table>
<tr><th colspan="2">V2.04</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description Contents</th><th>Page</th><th>Revised Contents</th></tr>
<tr><td>30</td><td>[11.1.3 Synchronous SRAM type transmission mode]<br> 

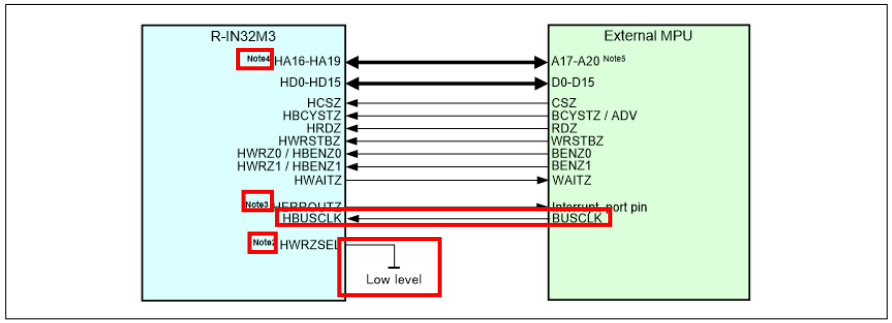
Figure 11.5 The connection example with external MPU (32bit bus, synchronous SRAM type transmission mode)<br> 

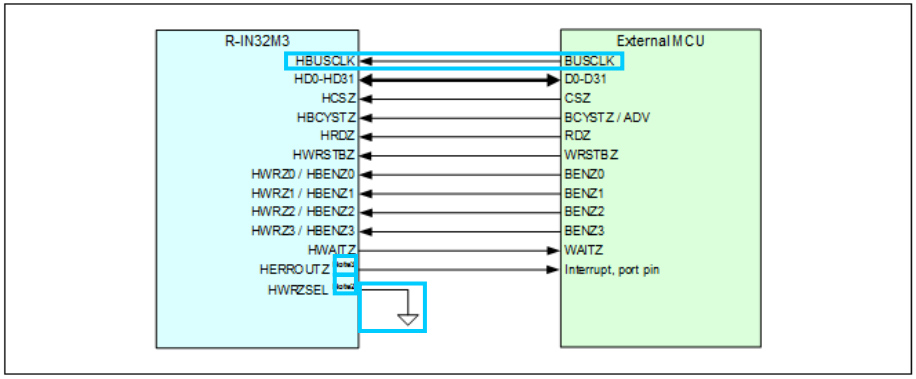
Figure 11.6 The connection example with external MPU (16bit bus, synchronous SRAM type transmission mode)</td><td>32</td><td>[11.1.3 Synchronous SRAM-Type Transfer Mode]<br> 

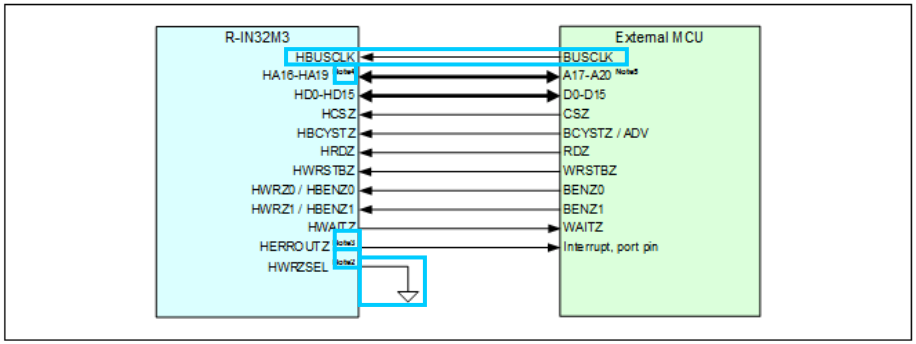
Figure 11.5 Connection Example of 32-Bit External MCU Interface (Synchronous SRAM-Type Transfer Mode)<br> 

Figure 11.6 Connection Example of 16-Bit External MCU Interface (Synchronous SRAM-Type Transfer Mode)</td></tr>
</table>

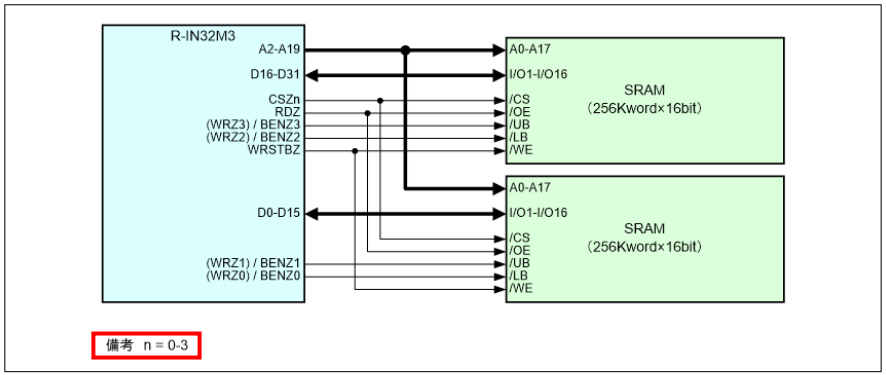
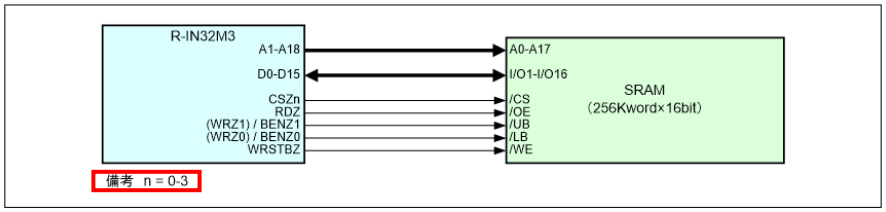
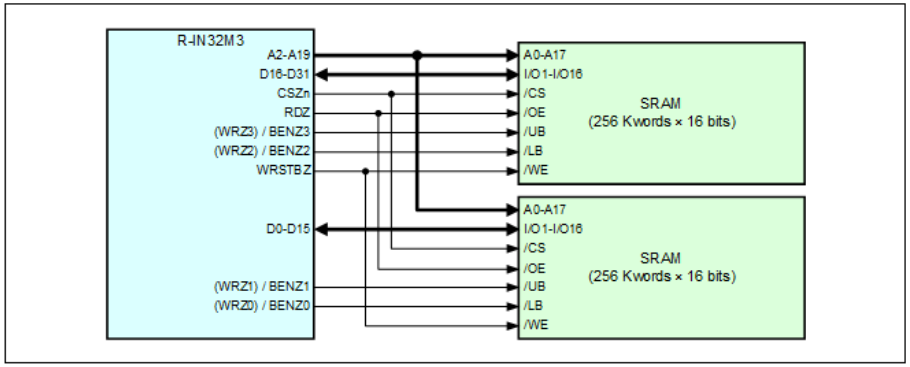
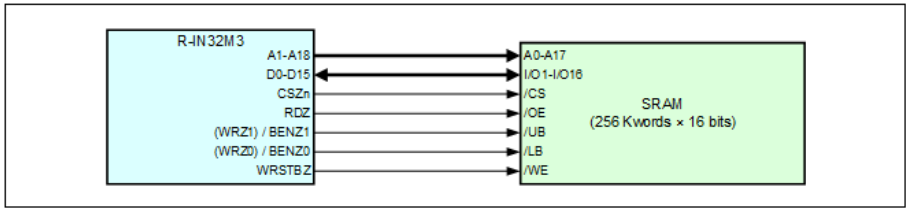
## No.22 11.2 External Memory Interface

**As it was not needed, the description on the MEMIFSEL pin was deleted.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 32 | **[11.2 External memory interface]**<br>This section describes about the connection to an external memory.<br>The connection mode of the external memory interface depends on the signal levels of the MEMCSEL pin and MEMIFSEL pin. (Please refer the Table 11.1.) | 34 | **[11.2 External Memory Interface]**<br>This section describes the connection as a master device to an external memory.<br>The operating connection mode of the external memory interface depends on the level of the signal on the MEMIFSEL pin (see Table 11.1). |

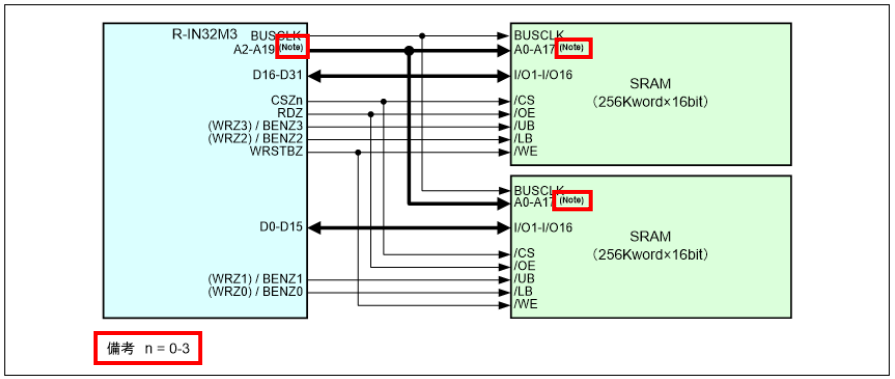
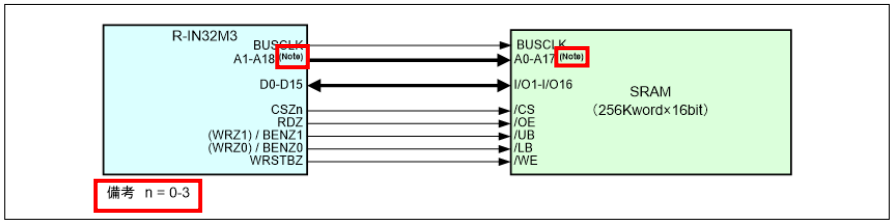
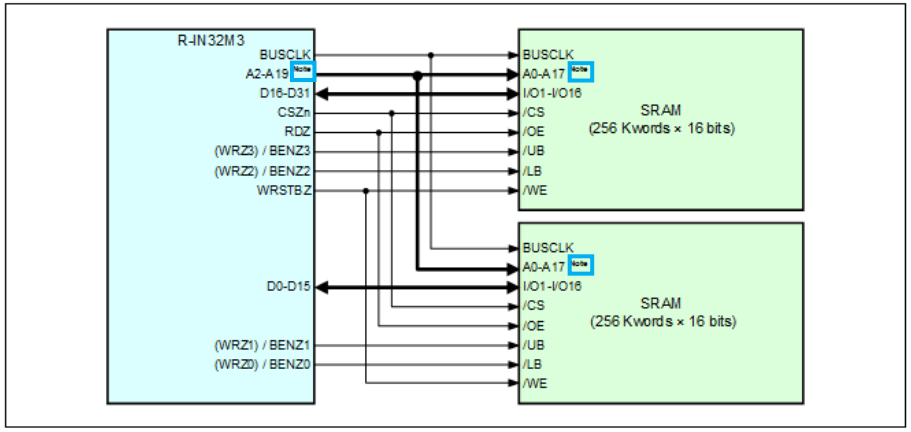
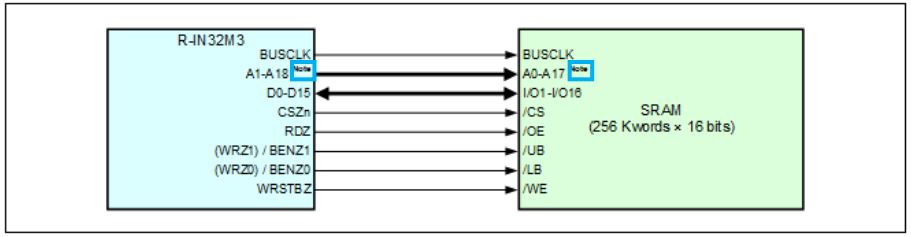
## No.23 11.2.1.1 Connection Example with SRAM

**Remarks in Figure 11.7 and Figure 11.8 were moved to outside of the figure frame.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 32 | **[11.2.1.1 SRAM connection example]**<br>  <br>Figure 11.7 Example of Connection with SRAM (32bit bus, asynchronous SRAM MEMC)<br>  <br>Figure 11.8 Example of Connection with SRAM (16bit bus, asynchronous SRAM MEMC) | 35 | **[11.2.1.1 Connection Example with SRAM]**<br>  <br>Figure 11.7 Connection Example with 32-Bit SRAM (Asynchronous SRAM MEMC)<br>  <br>Figure 11.8 Connection Example with 16-Bit SRAM (Asynchronous SRAM MEMC)<br>Remark n = 0 to 3 |

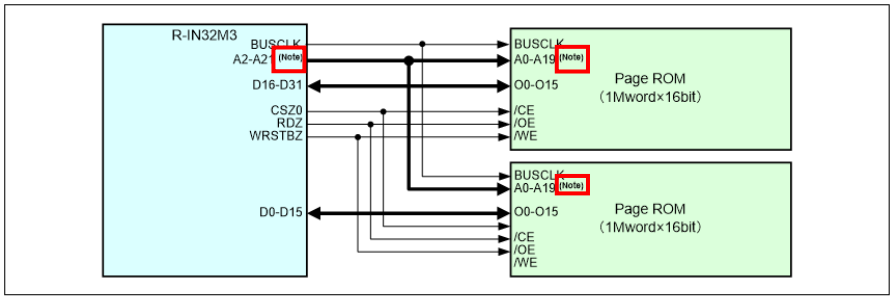
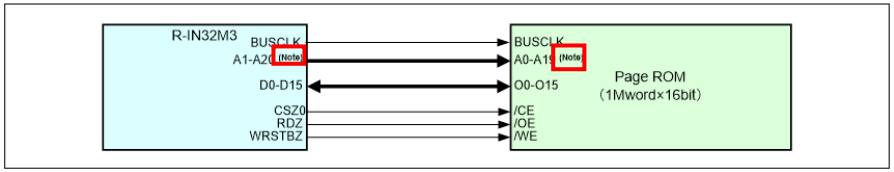
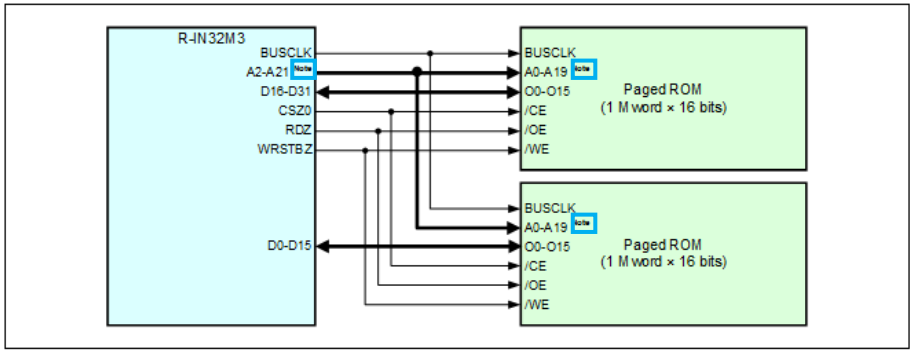
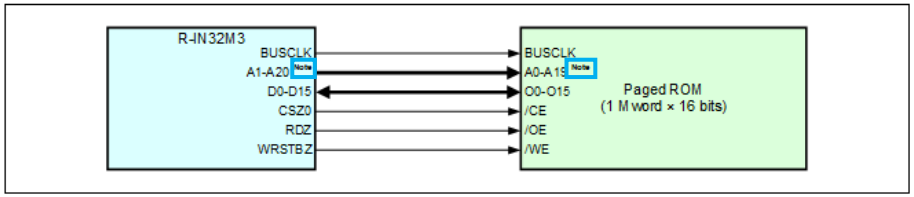
## No.24 11.2.2.1 Connection Example with SRAM

**Remarks in Figure 11.11 and Figure 11.12 were moved to outside of the figure frame. The description of Note was modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 34 | **[11.2.2.1 SRAM connection example]**<br>  <br>Figure 11.11 Example of Connection with SRAM (32bit bus, synchronous burst access MEMC)<br>  <br>Figure 11.12 Example of Connection with SRAM (16bit bus, synchronous burst access MEMC) | 35 | **[11.2.2.1 Connection Example with SRAM]**<br>  <br>Figure 11.11 Connection Example with 32-Bit SRAM (Synchronous Burst Access MEMC)<br>  <br>Figure 11.12 Connection Example with 16-Bit SRAM (Synchronous Burst Access MEMC)<br>Remark. n = 0 to 3 |

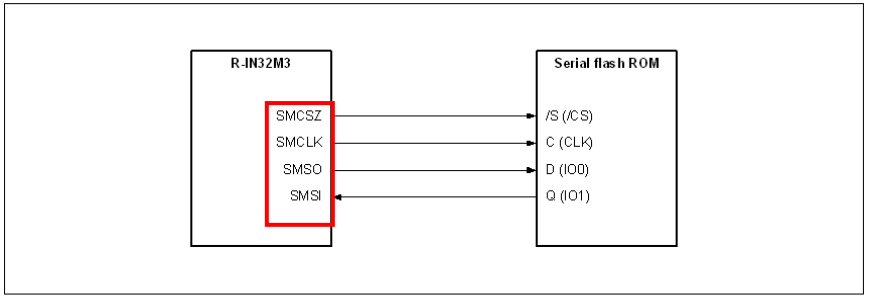
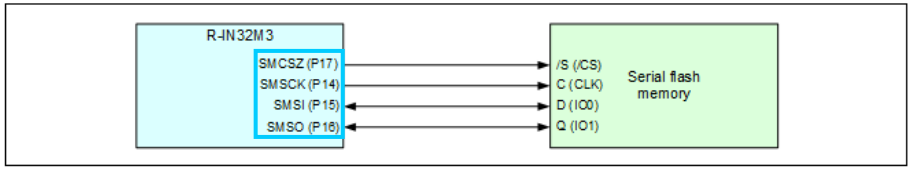
## No.25 11.2.2.2 Connection Example with Paged ROM

**The description of Note in Figure 11.13 and Figure 11.14 was modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 35 | **[11.2.2.2 Page ROM Connection Example]**<br>  <br>Figure 11.13 Example of Connection with Page ROM (32bit bus, synchronous burst access MEMC)<br>  <br>Figure 11.14 Example of Connection with Page ROM (16bit bus, synchronous burst access MEMC) | 36 | **[11.2.2.2 Connection Example with Paged ROM]**<br>  <br>Figure 11.13 Connection Example with 32-Bit Paged ROM (Synchronous Burst Access MEMC)<br>  <br>Figure 11.14 Connection Example with 16-Bit Paged ROM (Synchronous Burst Access MEMC) |

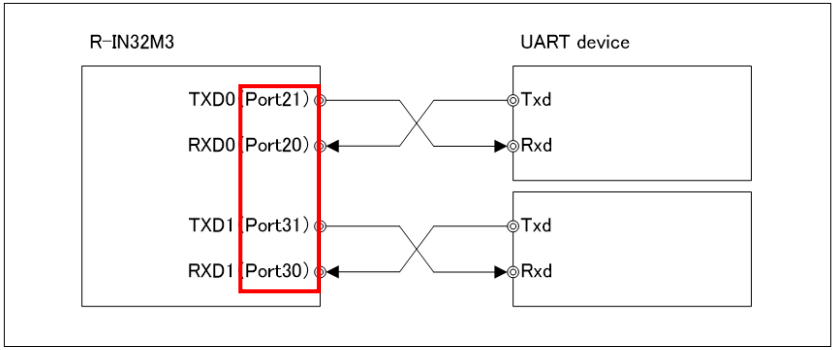
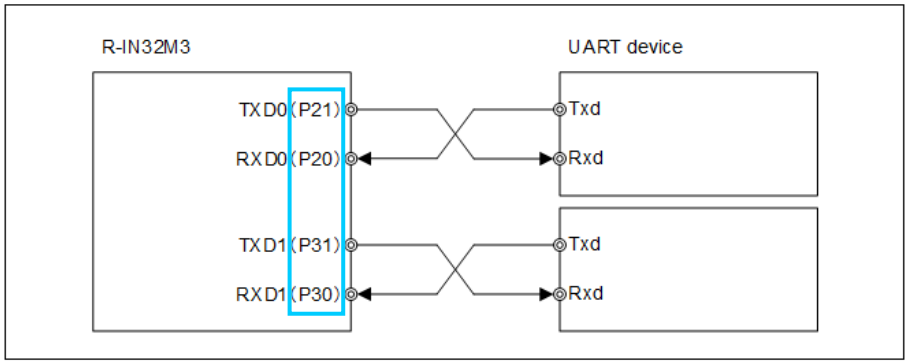
## No.26 12. Serial Flash ROM Connection Pins

**The name of port pin was added to the pin name in Figure 12.1.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 36 | **[12. Serial flash ROM connection pins]**<br>  <br>Figure 12.1 Connection with Serial Flash ROM | 37 | **[12. Serial Flash ROM Connection Pins]**<br>  <br>Figure 12.1 Connection Example with Serial Flash ROM |

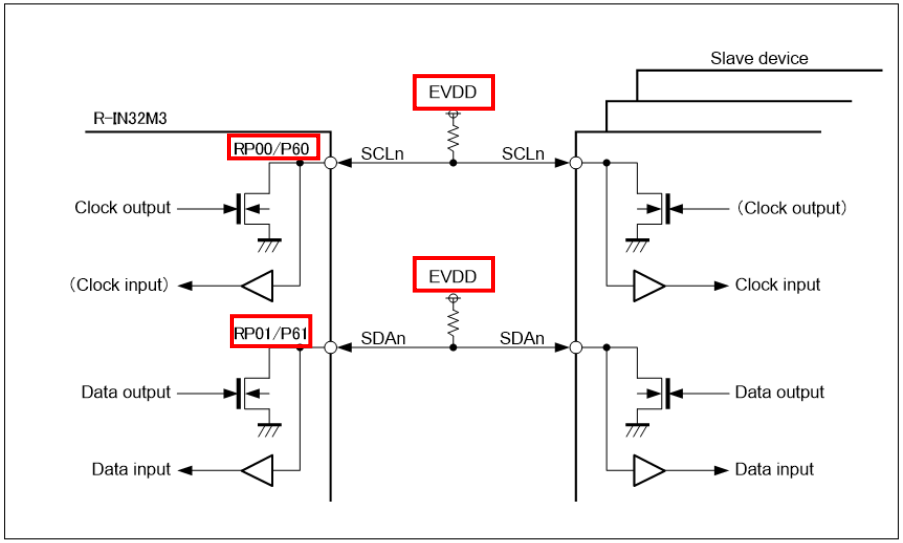
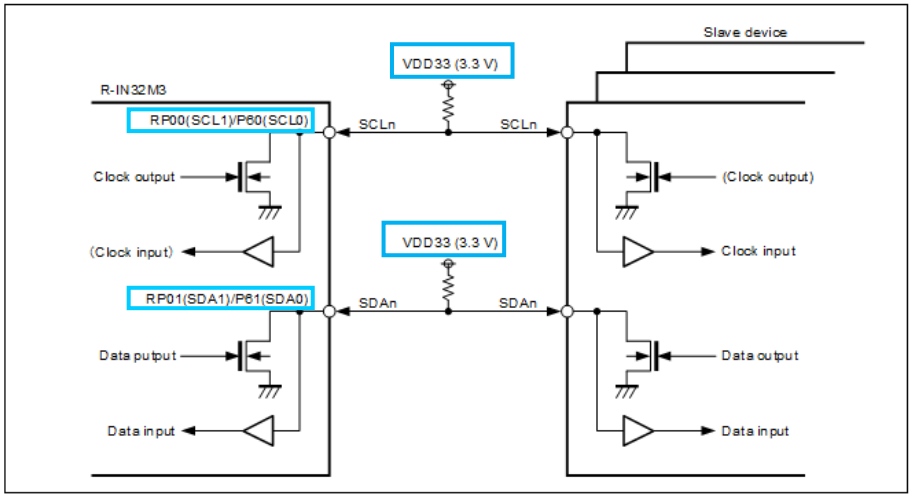
## No.27 13. Asynchronous Serial Interface J Connection Pins

**The section title was modified. The name of port pin was modified in Figure 13.1.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 37 | **[13. Asynchronous Serial Interface J(UARTJn) connection pins]**<br>Figure 13.1 shows a connection example between R-IN32M3 and Asynchronous Serial Interface J(UARTJn) device.<br>  <br>Figure 13.1 Connection example with the UART device | 38 | **[13. Asynchronous Serial Interface J Connection Pins]**<br>Figure 13.1 shows a connection example between the R-IN32M3 and the asynchronous serial interface J (UARTJn) device.<br>  <br>Figure 13.1 Connection Example between R-IN32M3 and UART Device |

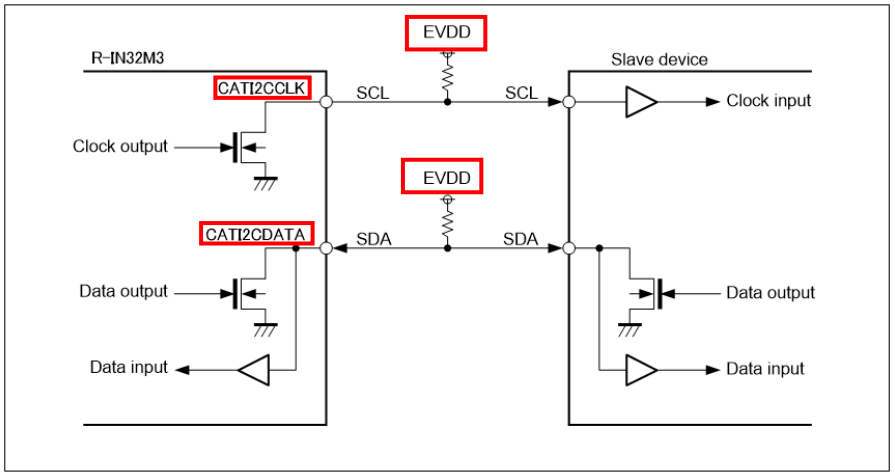
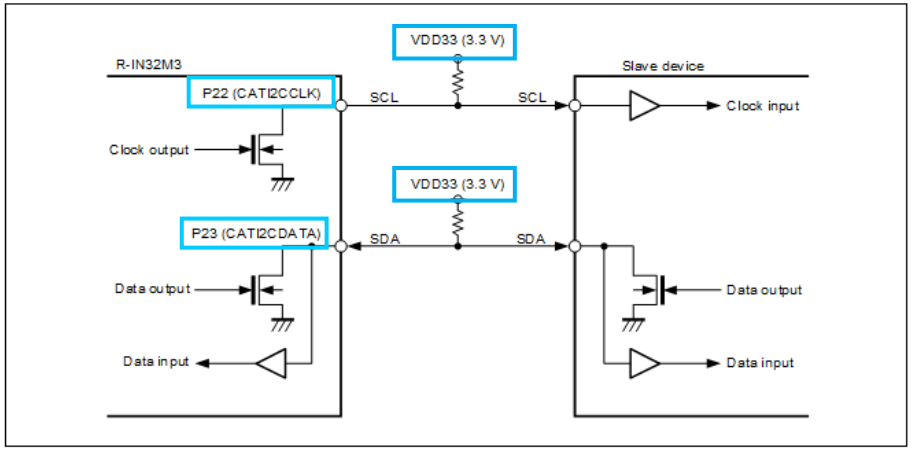
## No.28 14. I²C Connection Pins

**Pin handling in Figure 14.1 was modified. The name of I²C pin was added to the port pin.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 38 | **[14. I²C connection pins]**<br>  <br><br>Figure 14.1 Connection example with the I²C Slave device | 39 | **[14. I²C Connection Pins]**<br>  <br><br>Figure 14.1 Connection Example between R-IN32M3 and I²C Slave Device |

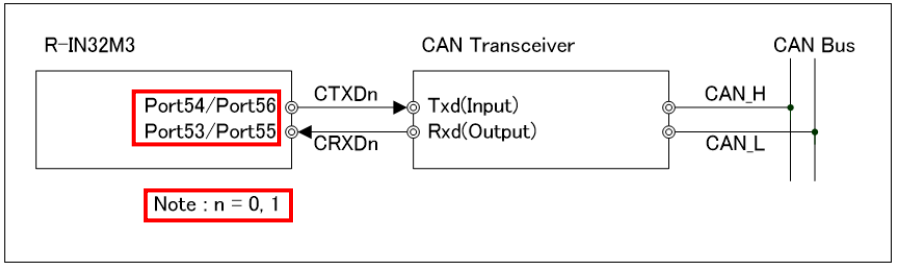
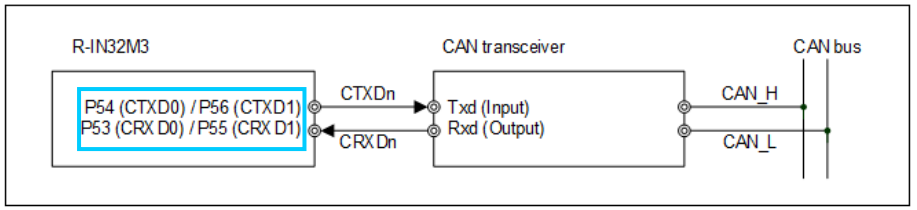
## No.29 15. EtherCAT EEPROM I2C Connection Pins (R-IN32M3-EC Only)

**The description of pin handling in Figure 15.1 was modified. The name of the multiplexing port was added to the EtherCAT pin.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 39 | **[15. EtherCAT EEPROM I²C connection pins (only R-IN32M3-EC)]**<br>  <br><br>Figure 15.1 Connection example with the EtherCAT EEPROM | 40 | **[15. EtherCAT EEPROM I²C Connection Pins (R-IN32M3-EC Only)]**<br>  <br><br>Figure 15.1 Connection Example between R-IN32M3-EC and EtherCAT EEPROM |

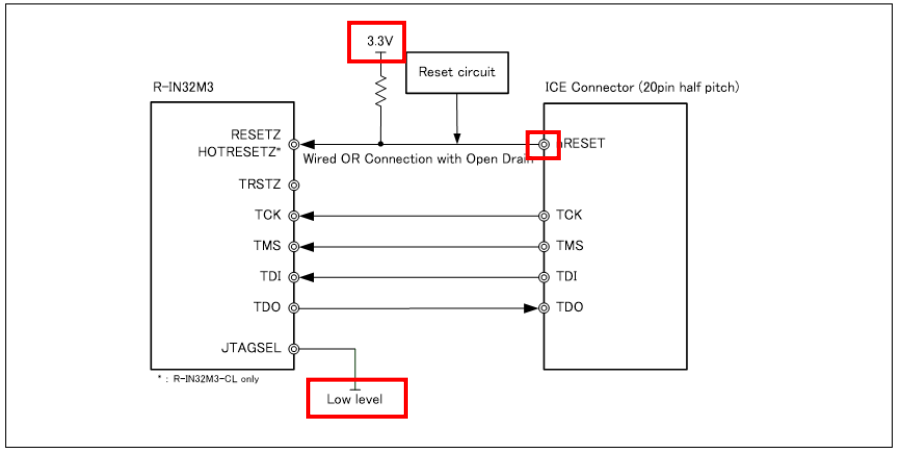
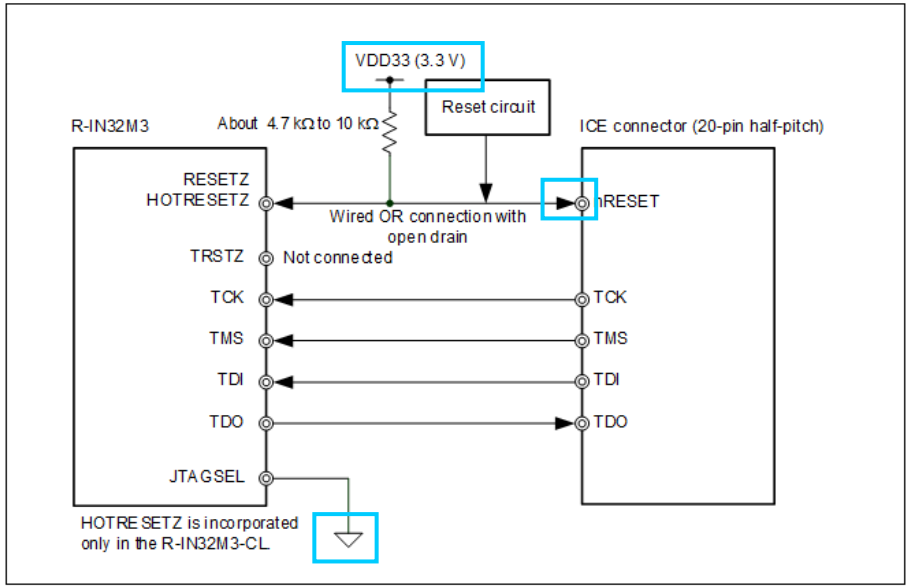
## No.30 16. CAN Pins

**The name of port pin was modified in Figure 16.1. The name of the CAN pin was added. Remark was moved to outside of the figure frame.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 40 | **[16. CAN pins]**<br>  <br>Figure 16.1 Connection example with the CAN Transceiver | 41 | **[16. CAN Pins]**<br>  <br>Figure 16.1 Connection Example between R-IN32M3 and CAN Transceiver<br>**Remark. n = 0 or 1** |

## No.31 17. JTAG/Trace Pins

**The connection of the ICE connector to the nRESET pin in Figure 17.1 was modified. Pin handling and the GND description were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 41 | **[17. JTAG/trace pins]**<br>  <br><br>Figure 17.1 JTAG interface connection example (20pin half pitch without trace) | 42 | **[17. JTAG/Trace Pins]**<br>  <br><br>Figure 17.1 Connection Example of JTAG Interface (20-Pin Half-Pitch without Trace) |

## No.32 17. JTAG/Trace Pins

**The connection of the ICE connector to the nRESET pin in Figure 17.2 was modified. The description on the wiring limitation was modified. Pin handling and the GND description were modified.**

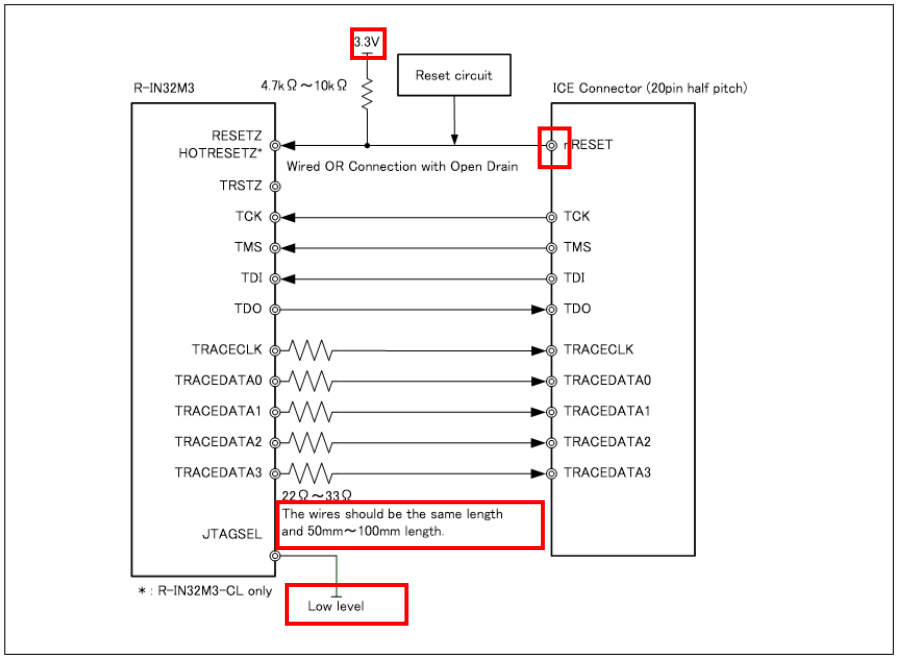
<table>
<tr><th colspan="2">V2.04</th><th colspan="2">V3.00</th></tr>
<tr><th>Page</th><th>Description Contents</th><th>Page</th><th>Revised Contents</th></tr>
<tr><td>42</td><td>[17. JTAG/trace pins]<br> 

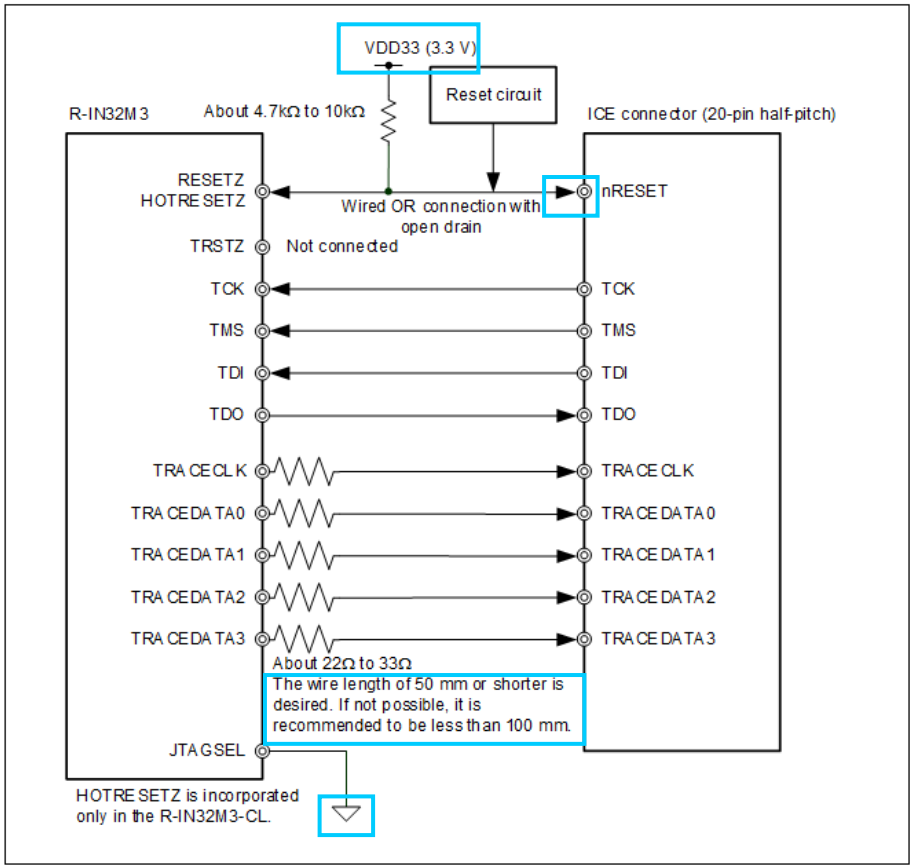
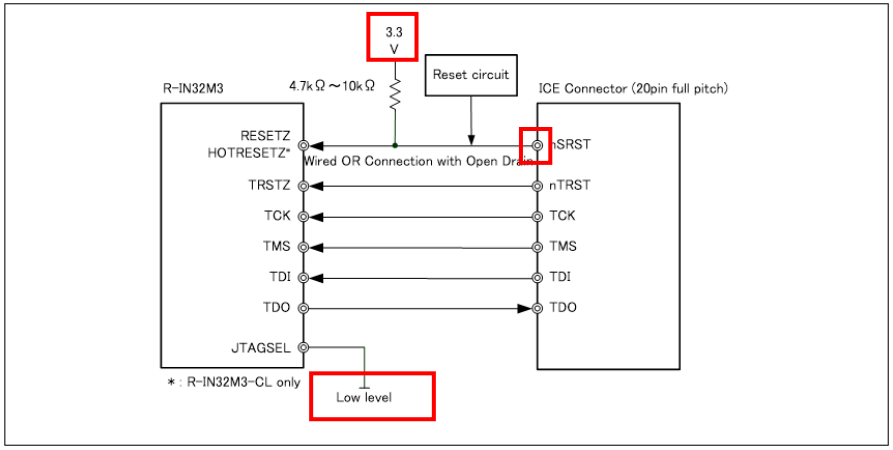
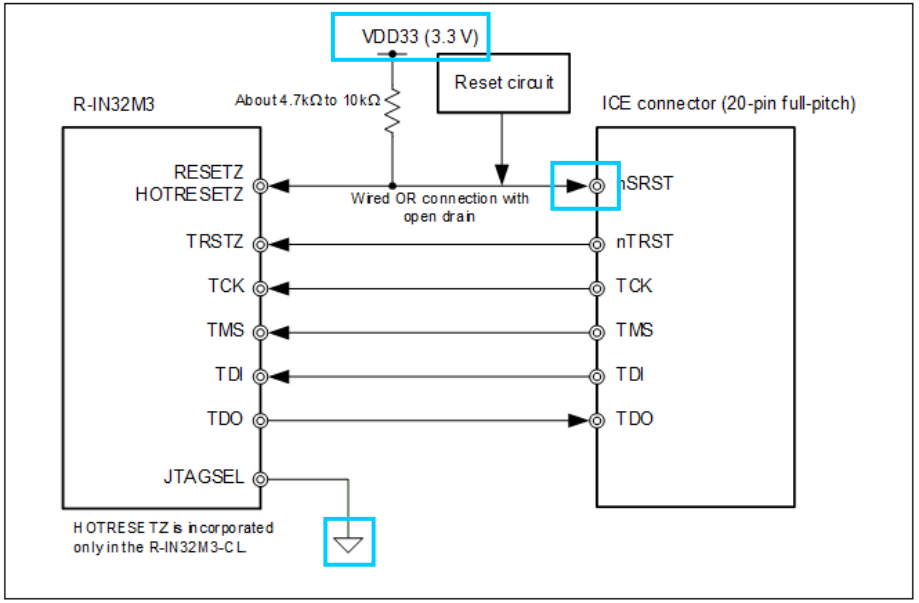
Figure 17.2 JTAG interface connection example (20pin half pitch with trace)</td><td>43</td><td>[17. JTAG/Trace Pins]<br> 

Figure 17.2 Connection Example of JTAG Interface (20-Pin Half-Pitch with Trace)</td></tr>
</table>

## No.33 17. JTAG/Trace Pins

**The connection of the ICE connector to the nRESET pin in Figure 17.3 was modified. Pin handling and the GND description were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 43 | **[17. JTAG/trace pins]**<br>  <br>Figure 17.3 JTAG interface connection example (20pin full pitch) | 44 | **[17. JTAG/Trace Pins]**<br>  <br>Figure 17.3 Connection Example of JTAG Interface (20-Pin Full-Pitch) |

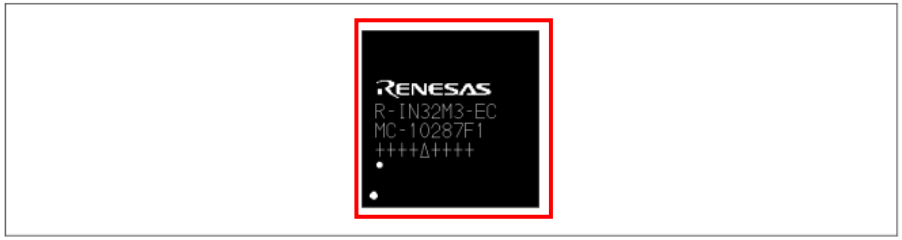
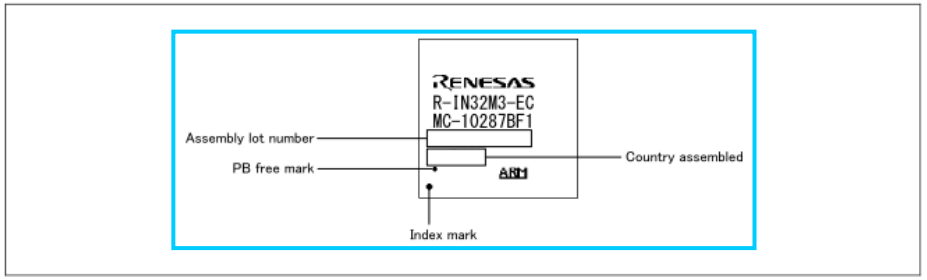
## No.34 22. IBIS Information

**The website was modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 50 | **[22. IBIS Information]**<br>Please obtaion from the following website IBIS information.<br>http://japan.renesas.com/products/soc/assp/fa_lsi/multi_protocol_communication/r-in32m3/peer/documents.jsp | 51 | **[22. IBIS Information]**<br>Please obtain the IBIS information from the following website.<br>https://www.renesas.com/products/factory-automation/multi-protocol-communication.html |

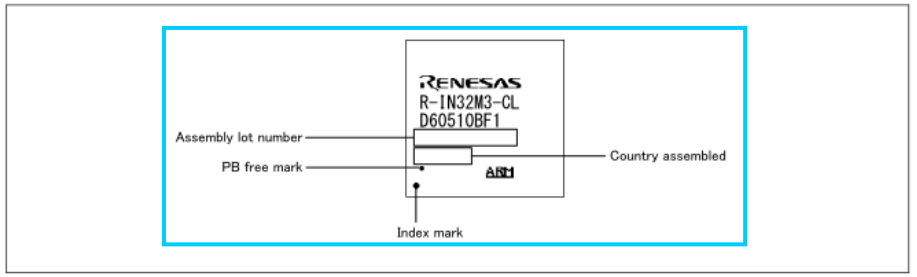
## No.35 23.1 R-IN32M3-EC

**The product name and the marking information of the R-IN32M3-EC were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 51 | **[23.1 R-IN32M3-EC]**<br>Product name: MC-10287F1-HN4-M1-A<br>  <br><br>Figure 23.1 R-IN32M3-EC Impress information | 52 | **[23.1 R-IN32M3-EC]**<br>Product name: MC-10287BF1-HN4-A, MC-10287BF1-HN4-M1-A<br>  <br><br>Figure 23.1 R-IN32M3-EC Marking Information |

## No.36 23.2 R-IN32M3-CL

**The product name and the marking information of the R-IN32M3-CL were modified.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| 51 | **[23.2 R-IN32M3-CL]**<br>Product name: UPD60510F1-HN4-M1-A<br>  <br><br>Figure 23.2 R-IN32M3-CL Impress information | 52 | **[23.2 R-IN32M3-CL]**<br>Product name: UPD60510BF1-HN4-A, UPD60510BF1-HN4-M1-A<br>  <br><br>Figure 23.2 R-IN32M3-CL Marking Information |

## No.37 24. Guide to Thermal Design

**The guide to the thermal design for the R-IN32M3-EC was newly added.**

| V2.04 | | V3.00 | |
|---|---|---|---|
| Page | Description Contents | Page | Revised Contents |
| - | (Not described) | 53 to 61 | **[24. Guide to Thermal Design]** |