Date: Jun. 19, 2024

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0136B/E	Rev.	2.00
Title	Notification of Corrections to Errors Amendments to Descriptions and Limitations on the Capacitive Sensing Unit		Information Category	Technical Notification		
Applicable Product	RL78/G22 Group and RL78/G23 Group	Lot No. All lots	Reference Document	RL78/G22 User's Manual: Hardware Rev. 1.00 R01UH0978EJ0100 (Dec. 2022) RL78/G23 User's Manual: Hardware Rev. 1.30 R01UH0896EJ0130 (Jan. 2024)		

1. Corrections to Errors

The following errors in Revision 1.00 of the RL78/G22 User's Manual: Hardware (R01UH0978EJ0100) and Revision 1.30 of the RL78/G23 User's Manual: Hardware (R01UH0896EJ0130) are to be corrected.

Corrections

Applicable Item	Applicable Page		Contents
	R01UH0978 EJ0100 (RL78/G22)	R01UH0896 EJ0130 (RL78/G23)	
Sensor Drive Pulse Output Clock Configuration	Page 1005	Page 1255	Incorrect descriptions revised
CTSU control registers AL and AH (CTSUCRAL, CTSUCRAH)	Page 1008 to Page 1010	Page 1259 to Page 1261	Incorrect descriptions revised
CTSU status register L (CTSUSRL)	Page 1026	Page 1276	Incorrect descriptions revised
CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)	Page 1027	Page 1277	Incorrect descriptions revised
CTSU sensor unit clock control registers AL, AH, BL, and BH (CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, CTSUSUCLK3)	Page 1033, Page 1034	Page 1283, Page 1284	Incorrect descriptions revised
CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)	Page 1035	Page 1285	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

2. Effects of the Errors on Applicable Products

In descriptions of the capacitive sensing unit in the user's manuals for the applicable products stated above, SUCLK frequencies that are outside the range at which SUCLK is capable of operating are included. Setting an SUCLK frequency that is outside this range according to the erroneous descriptions may lead to an incorrect result of touch measurement.

However, if the QE (Quick and Effective Tool Solution) for Capacitive Touch tool V3.3.0, a development assistance tool for capacitive touch sensors, is in use and multi-frequency measurement is selected (the default setting), majority decision will proceed. Accordingly, the final result of touch measurement is considered unlikely to be incorrect in such cases. See 2.1, Effects on Touch Detection for details.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items					Pages in this document for corrections
		Document No.	English	R01UH0978 EJ0100 (RL78/G22)	R01UH0896 EJ0130 (RL78/G23)	
1.1	Sensor Drive Pulse Output Clock Configuration			Page 1005	Page 1255	Page 3
1.2	CTSU control registers AL and AH (CTSUCRAL, CTSUCRAH)			Page 1008 to Page 1010	Page 1259 to Page 1261	Page 4 to Page 6
1.3	CTSU status register L (CTSUSRL)			Page 1026	Page 1276	Page 7
1.4	CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)			Page 1027	Page 1277	Page 8
1.5	CTSU sensor unit clock control registers AL, AH, BL, and BH (CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, CTSUSUCLK3)			Page 1033, Page 1034	Page 1283, Page 1284	Page 9, Page 10
1.6	CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)			Page 1035	Page 1285	Page 11

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G22 and RL78/G23 Correction for incorrect description notice

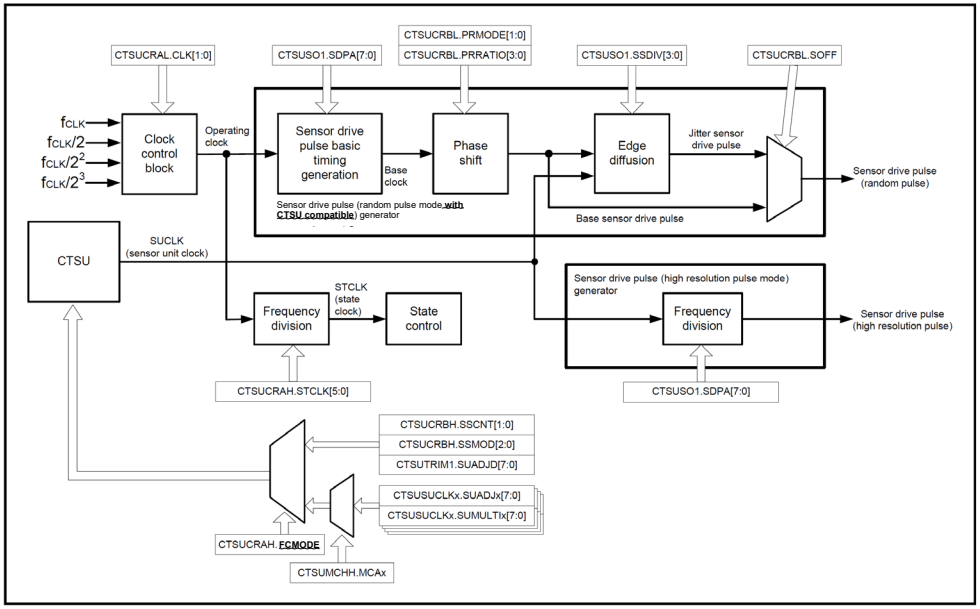
Document Number	Issue Date	Rev.	Description
TN-RL*-A0136A/E	May 28, 2024	1.00	First edition issued
TN-RL*-A0136B/E	Jun. 19, 2024	2.00	Regarding page 6, the register symbols were corrected. Regarding page 9, "SUCLK Multiplication Rate Setting" was corrected to "STCLK Multiplication Rate Setting".

1.1 Sensor Drive Pulse Output Clock Configuration

Incorrect:

Page 1005 (RL78/G22), Page 1255 (RL78/G23)

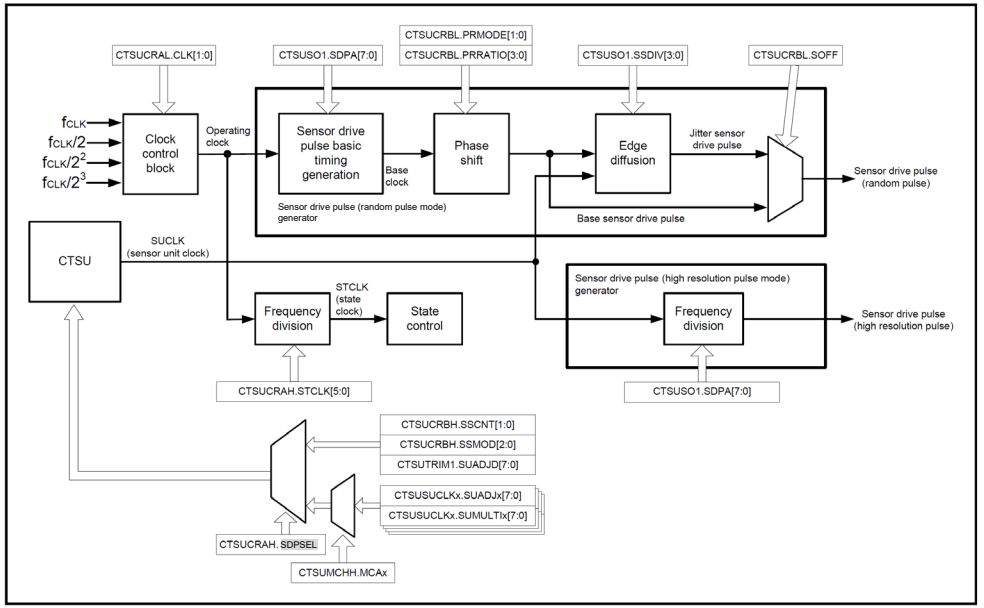
(omitted)



(omitted)

Correct:

(omitted)



(omitted)

1.2 CTSU control registers AL and AH (CTSUCRAL, CTSUCRAH)

Incorrect:

Page 1008 (RL78/G22), Page 1259 (RL78/G23)

(omitted)

Address: F0500H, F0501H (CTSUCRAL), F0502H, F0503H (CTSUCRAH)
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
CTSUCRAH	DCBACK	DCMODE	STCLK[5:0]					

	7	6	5	4	3	2	1	0
	FCMODE	SDPSEL	POSEL[1:0]		LOAD1	LOAD0	ATUNE2	0

Correct:

(omitted)

Address: F0500H, F0501H (CTSUCRAL), F0502H, F0503H (CTSUCRAH)
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
CTSUCRAH	DCBACK	DCMODE	STCLK[5:0]					

	7	6	5	4	3	2	1	0
	PCSEL	SDPSEL	POSEL[1:0]		LOAD1	LOAD0	ATUNE2	0

Page 1009 (RL78/G22), Page 1260 (RL78/G23)

(omitted)

FCMODE	Sensor unit clock (SUCLK) Select
0	SUCLK is used as frequency diffusion clock.
1	SUCLK is used as recovery clock for multi-clock measurement. To use SUCLK as recovery clock, set the CTSUDBGR1.CCOCLK bit to 1.

- When the FCMODE bit is 0 (SUCLK used as frequency diffusion clock)

  As specified in the CTSUTRIM1.SUADJD[7:0], CTSUCRBH.SSCNT[1:0], and CTSUCRBH.SSMOD[2:0],
  SUCLK is generated when the digital oscillator oscillates and the frequency is spectrum-diffused.

- When the FCMODE is 1 (SUCLK used as recovery clock for multi-clock measurement)

  As specified in the CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, or CTSUSUCLK3 register, SUCLK is generated when the clock recovery control is performed.
  Before setting the FCMODE bit to 1, set the CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, or CTSUSUCLK3 register.
  The recovery is performed in status 0 (non-measurement state) for all selected clocks during measurement. The SUADJx bits in the CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, or CTSUSUCLK3 register are updated by recovery (x = 0 to 3).
  When the FCMODE bit is 1, do not change the CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, or CTSUSUCLK3 register setting.

<Relationship between SDPSEL and FCMODE>

SDPSEL	FCMODE	Operation
0	0	Random pulse mode (CTSU compatible setting)
1	1	Sensor unit clock (SUCLK) mode Used for multi-clock measurement
Other than above		Setting prohibited

(omitted)

PCSEL	Voltage Booster Clock Select
0	Sensor drive pulse
1	STCLK
This bit selects the clock for the voltage boost circuit.	

Page 1010 (RL78/G22), Page 1261 (RL78/G23)

SDPSEL	Sensor Drive Pulse Select
0	Random pulse mode (CTSU compatible setting) The operating clock divided by the settings of the CTSUSO1.SDPA[7:0] bits is used as the base clock, and the sensor drive pulse is obtained by phase-shifting the base clock using the random number generated according to the settings of the CTSUCRBL.PRMODE[1:0] and CTSUCRBL.PRRATIO[3:0] bits. It is also possible to apply jitter by the frequency diffusion clock.
1	Sensor unit clock (SUCLK) mode The sensor drive pulse is obtained by applying frequency recovery based on fCLK to generate SUCLK and dividing it by the settings of the CTSUSO1.SDPA[7:0] bits.
The SDPSEL bit selects the sensor drive pulse.	

(omitted)

SDPSEL	Sensor Drive Pulse and SUCLK Select
0	Random pulse mode ● Sensor drive pulse f_{CLK} divided by the settings of the CTSUCRAL.CLK[1:0] and CTSUSO1.SDPA[7:0] bits are used as the base clock, and the sensor drive pulse is obtained by phase-shifting the base clock using the random number generated according to the settings of the CTSUCRBL.PRMODE[1:0] and CTSUCRBL.PRRATIO[3:0] bits. It is also possible to apply jitter by the frequency diffusion clock. ● SUCLK The built-in oscillator is operated with the settings of CTSUCRBH.SSCNT[1:0], CTSUCRBH.SSMOD[2:0], and CTSUTRIM1.SUADJD[7:0] to generate SUCLK with frequency spread spectrum.
1	Hi-resolution pulse mode ● Sensor drive pulse The clock (base clock) obtained by dividing SUCLK by the CTSUSO1.SDPA[7:0] bits is used as the sensor drive pulse. ● SUCLK By setting the CTSUSUCLKx register (x = 0 to 3), clock recovery control is performed and SUCLK is generated. Recovery updates the CTSUSUCLKx.SUADJx[7:0] bits. Set the CTSUSUCLKx register before setting this bit to 1. Do not change the CTSUSUCLKx register while this bit is 1.
The SDPSEL bit toggles between random pulse mode and hi-resolution pulse mode. This selection changes how the sensor drive pulse and SUCLK are generated.	

(omitted)

1.3 CTSU status register L (CTSUSRL)

Incorrect:

Page 1026 (RL78/G22), Page 1276 (RL78/G23)

(omitted)

MFC[1:0]		Multi-clock Counter
0	0	Multi-clock 0
0	1	Multi-clock 1
1	0	Multi-clock 2
1	1	Multi-clock 3
The MFC[1:0] bits indicate the clock that is being measured during multi-clock measurement (CTSUCRAH.**FCMODE** = 1).		

Correct:

(omitted)

MFC[1:0]		Multi-clock Counter
0	0	Multi-clock 0
0	1	Multi-clock 1
1	0	Multi-clock 2
1	1	Multi-clock 3
The MFC[1:0] bits indicate the clock that is being measured during multi-clock measurement (CTSUCRAH.SDPSEL = 1).		

1.4 CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)

Incorrect:

Page 1027 (RL78/G22), Page 1277 (RL78/G23)

(omitted)

SDPA[7:0]	Sensor Driving Pulse Divisor Setting

• When CTSUCRAH.SDPSEL = 0

The operating clock is divided to generate a base clock to be the source of sensor drive pulse. These bits are also available for setting the voltage stabilization time of the CTSU.

0	0	0	0	0	0	0	0	Operating clock divided by 2Note
0	0	0	0	0	0	0	1	Operating clock divided by 4
0	0	0	0	0	0	1	0	Operating clock divided by 6
0	0	0	0	0	0	1	1	Operating clock divided by 8
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	Operating clock divided by 510
1	1	1	1	1	1	1	1	Operating clock divided by 512

Note When jitter application is disabled (CTSUCRBL.SOFF bit = 1) in the mutual capacitance method, setting of SDPA[7:0] = 00000000B is prohibited.

• When CTSUCRAH.SDPSEL = 1

The SUCLK clock is divided to generate a sensor drive pulse.

0	0	0	0	0	0	0	0	SUCLK divided by 1
0	0	0	0	0	0	0	1	SUCLK divided by 2
0	0	0	0	0	0	1	0	SUCLK divided by 3
0	0	0	0	0	0	1	1	SUCLK divided by 4
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	SUCLK divided by 255
1	1	1	1	1	1	1	1	SUCLK divided by 256

Correct:

(omitted)

SDPA[7:0]	Base Clock (Sensor Drive Pulse Frequency Divisor) Setting

• For the random pulse mode, that is, when CTSUCRAH.SDPSEL = 0.

The operating clock is divided to generate a base clock to be the source of sensor drive pulse. These bits are also available for setting the voltage stabilization time of the CTSU. If the setting of the CTSUSO1.SDPA[7:0] bits is n, the base clock is obtained by frequency-dividing the operating clock by 2(n+1).

0	0	0	0	0	0	0	0	Operating clock divided by 2Note
0	0	0	0	0	0	0	1	Operating clock divided by 4
0	0	0	0	0	0	1	0	Operating clock divided by 6
0	0	0	0	0	0	1	1	Operating clock divided by 8
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	Operating clock divided by 510
1	1	1	1	1	1	1	1	Operating clock divided by 512

Note When jitter application is disabled (CTSUCRBL.SOFF bit = 1) in the mutual capacitance method, setting of SDPA[7:0] = 00000000B is prohibited.

• For the hi-resolution pulse mode, that is, when CTSUCRAH.SDPSEL = 1.

The SUCLK clock is divided to generate a sensor drive pulse.

The SUCLK frequency can be calculated from the following expression.

SUCLK = STCLK ×SUCLK multiplication rate setting made by the CTSUSUCLKx.SUMULTIx[7:0] bits

If the setting of the CTSUSO1.SDPA[7:0] bits is n, the sensor drive pulses are obtained by frequency-dividing the SUCLK clock by 2(n+1).

0	0	0	0	0	0	0	0	SUCLK divided by 2
0	0	0	0	0	0	0	1	SUCLK divided by 4
0	0	0	0	0	0	1	0	SUCLK divided by 6
0	0	0	0	0	0	1	1	SUCLK divided by 8
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	SUCLK divided by 510
1	1	1	1	1	1	1	1	SUCLK divided by 512

1.5 CTSU sensor unit clock control registers AL, AH, BL, and BH (CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, CTSUSUCLK3)

Incorrect:

Page 1033 (RL78/G22), Page 1283 (RL78/G23)

(omitted)

SUMULTIx[7:0]	**SUCLK** Multiplication Rate Setting

The SUMULTIx[7:0] bits set the multiplication rate of STCLK (assuming 0.5 MHz (divided f_{CLK})) to generate SUCLK.

STCLK is compared with SUCLK divided by this setting. Based on the comparison result, the SUADJx[7:0] bits are updated. The target clock frequency is 32 to 80 MHz.

0	0	0	0	0	0	0	0	× 1
:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	× 64
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	× 128
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	× 256

Correct:

(omitted)

SUMULTIx[7:0]	STCLK Multiplication Rate Setting

The SUMULTIx[7:0] bits set the frequency multiplier for generating SUCLK from STCLK (which is taken to be at 0.5 MHz, obtained by frequency-dividing f_{CLK}).

The SUCLK clock is capable of operating at a frequency in the range from 16 MHz to 32 MHz.

If the SUCLK clock is to be used, ensure that its frequency is within that range.

In addition, the SUADJx[7:0] bits are updated in response to the SUCLK frequency generated by this setting.

The SUCLK frequency can be calculated from the following expression.

SUCLK = STCLK ×SUCLK multiplication rate setting made by the CTSUSUCLKx.SUMULTIx[7:0] bits

0	0	0	0	0	0	0	0	× 1
:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	× 64
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	× 128
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	× 256

Page 1034 (RL78/G22), Page 1284 (RL78/G23)

SUADJx[7:0]	SUCLK Frequency Adjustment
The SUADJx[7:0] bits set the initial value of the SUCLK frequency. **The drift is adjusted and the SUADJx[7:0] value is updated by the clock recovery function.** **The output frequency varies from the set value in each MCU. The SUCLK frequency is adjusted based on the register set value as an initial value and the register value is updated by the clock recovery control.**	

SUADJx[7:0]	SUCLK Frequency Adjustment
The SUADJx[7:0] bits set the initial value of the SUCLK frequency. The clock recovery function corrects SUCLK for clock drift, resulting in updating of this register value. Do not write values to these registers.	

1.6 CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)

Incorrect:

Page 1035 (RL78/G22), Page 1285 (RL78/G23)

(omitted)

SUADJD[7:0]	SUCLK Frequency Adjustment
The SUADJD[7:0] bits hold the initial value for generating approx. 64 MHz, which is set at the factory. When FCMODE is 0, this set value is input to the digital oscillator. Do not modify this initial value set at the factory.	

(omitted)

Correct:

(omitted)

SUADJD[7:0]	SUCLK Frequency Adjustment
The SUADJD[7:0] bits are used to adjust the SUCLK frequency in the random pulse mode (selected by CTSUCRAH.SDPSEL = 0). These bits hold the initial setting at the time of shipment. Do not write values to them.	

(omitted)

2.1 Effects on Touch Detection

2.1.1 Problem

The usable range of SUCLK frequency is stated to be 32 MHz to 80 MHz, but the range of frequency at which SUCLK is actually capable of operating is 16 MHz to 32 MHz. Proceeding with touch measurement with the SUCLK frequency set to a value outside the range from 16 MHz to 32 MHz may lead to the result of touch detection in the first cycle of SUCLK being undefined. This is likely to result in an error of ± 1 being generated in the value of the counter for the results of touch measurement. The effect of this on the results of touch measurement is considered to be negligible.

2.1.2 Workaround for the Problem

The SUCLK frequency is determined by the following expression. Set the CTSUCRAL.CLK[1:0], CTSUCRAH.STCLK[5:0], and CTSUSUCLK0 and CTSUSUCLK1.SUMULTIx[7:0] bits so that the SUCLK frequency is in the range from 16 MHz to 32 MHz.

SUCLK = (f_{CLK} frequency/CLK/STCLK) × SUMULTIx setting

CLK above refers to the CTSUCRAL.CLK[1:0] setting. f_{CLK} is frequency-divided by the value corresponding to this setting in setting the operating clock.

STCLK above refers to the CTSUCRAH.STCLK[5:0] setting. The operating clock is frequency-divided by the value corresponding to this setting in setting the state clock (STCLK).

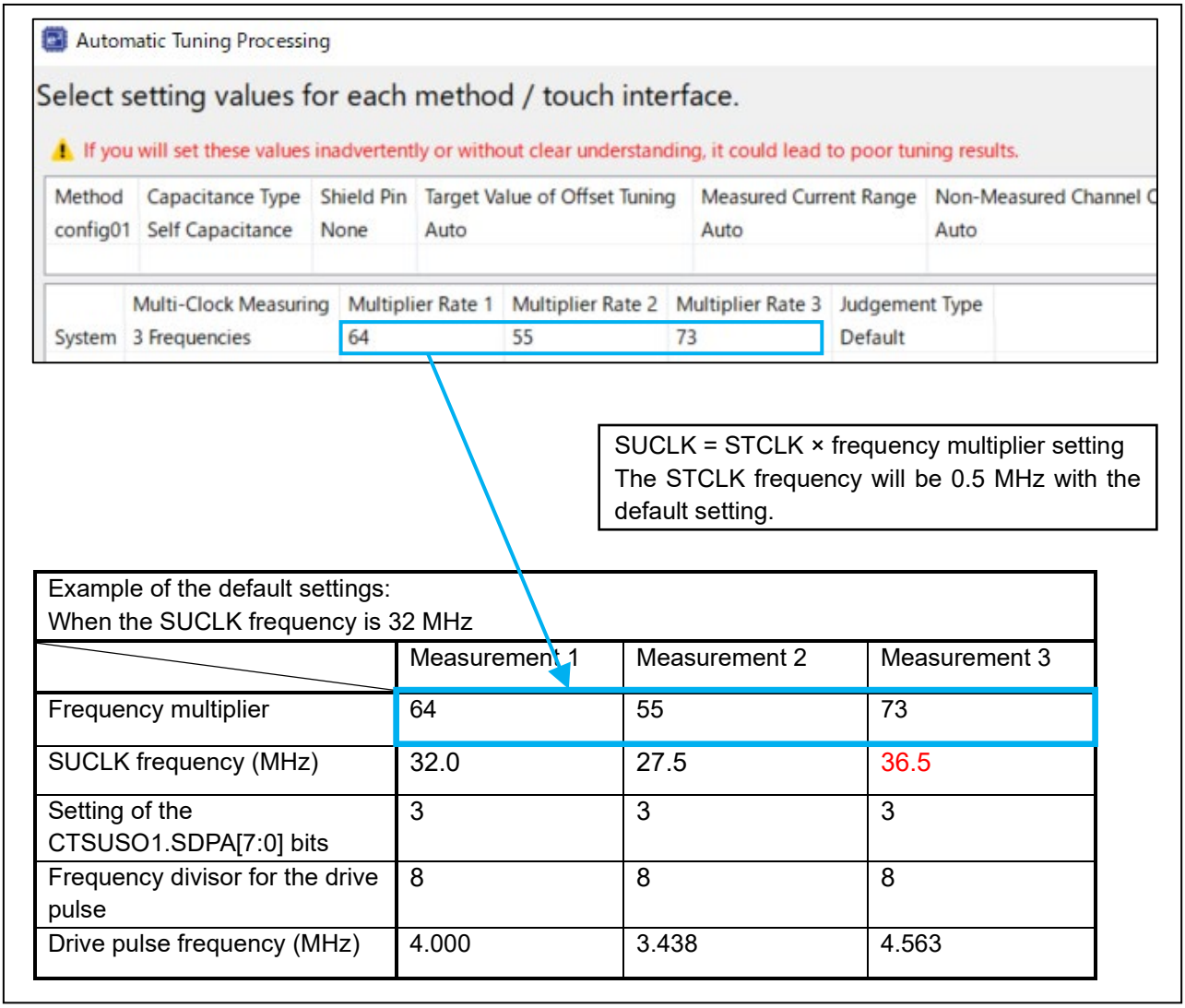
SUMULTIx above refers to the CTSUSUCLK0 or CTSUSUCLK1.SUMULTIx[7:0] setting. STCLK is multiplied by the value corresponding to this setting in setting SUCLK.

2.1.3 Effects When the QE for Capacitive Touch Tool V3.3.0, a Development Assistance Tool for Capacitive Touch Sensors, Is in Use

Use of the QE for Capacitive Touch tool, a development assistance tool for capacitive touch sensors, allows the setting of the SUCLK frequency to a value outside the permissible frequency range for SUCLK operation.

Figure 2-1 shows the default settings of the QE tool V3.3.0, which select three-frequency measurement.
Using the SIS driver (an RL78 touch driver) for the CTSU module enables multi-frequency measurement. With the default settings, three-frequency measurement proceeds. Specifically, three frequencies, n, (n-x), and (n+x) MHz, are used for measurement and majority decision proceeds.
With the default settings of the QE tool V3.3.0, the SUCLK frequency for measurement 3 is 36.5 MHz, which is outside the permissible frequency range for SUCLK operation, as indicated by the red text in Figure 2-1.
Setting the frequency to 36.5 MHz may lead to an error of ± 1 being generated in the value of the counter for the results of touch measurement.
However, the final result of touch measurement is considered unlikely to be incorrect because majority decision proceeds in multi-frequency measurement. Corrections concerning this problem will be made in the next revision of the QE tool.
In addition, setting a frequency greater than 32 MHz does not create a risk of damage to the microcontroller.

Figure 2-1 Settings of the QE Tool V3.3.0 for Three-Frequency Measurement (the Default Settings)



Example of the default settings:
When the SUCLK frequency is 32 MHz

	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	64	55	73
SUCLK frequency (MHz)	32.0	27.5	36.5
Setting of the CTSUSO1.SDPA[7:0] bits	3	3	3
Frequency divisor for the drive pulse	8	8	8
Drive pulse frequency (MHz)	4.000	3.438	4.563