

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A719A/E	Rev.	1.00
Title	Notice about the flag bit of DMAC, BSC, SIO and SIOF (SH7670 Group, SH7619 Group, SH7615 Group, SH7616 Group)		Information Category	Technical Notification		
Applicable Product	SH7670 Group SH7619 Group SH7615 Group SH7616 Group	Lot No.	Reference Document	SH7670 Group Hardware Manual Rev.2.00 (REJ09B0437-0200) SH7619 Group Hardware Manual Rev.5.00 (REJ09B0237-0500) SH7615 Group Hardware Manual Rev. 2.00 (REJ09B0157-0200O) SH7616 Hardware Manual Rev. 2.00 (REJ09B0292-0200)		
		All				

We would like to inform you of two notices regarding flag bits of DMAC, BSC, SIO and SIOF as described below.

[Notice 1]

This notice applies flag bits listed in table 1.

Table 1

Module	Register	Bit Name	Applicable Product
DMAC	DMA Channel Control Registers (CHCR)	HE(Half-End Flag)	SH7670 Group
		TE(Transfer End Flag)	SH7670 Group
	DMA Operation Register (DMAOR)	AE(Address Error Flag)	SH7619 Group
BSC	Refresh Timer Control/Status Register (RTCSR)	CMF(Compare Match Flag)	SH7615 Group SH7616 Group

Just when a flag is set to 1, if the flag is read, the read data will be 0, but the internal state will be the same as reading 1.

In that case, if the flag is written 0, the flag will be cleared as 0, because the internal state is the same as reading 1.

[Workaround for Notice 1]

In the case of using a flag of DMAC and BSC, to protect unintended bit clear to 0, please write it as following.

- 1) In the case of intended bit clear, please write 0 after reading 1 to the flag.
- 2) In the other cases, please write 1 to the flag.

If the flag is not used, it is no problem to write 0 to flag (in the case of intended bit clear, write 0 after reading 1 to the flag).

If an interrupt is generated by the flag and the flag causing the interrupt is read in an interrupt handler routine, this case does not apply to the notice 1. However if there is a possibility that another flag bit in the register is set at the timing of reading the register, please follow the workaround described above.

[Notice 2]

This notice applies flag bits listed in table 2.

Table 2

Module	Register	Bit Name	Applicable Product
SIO	Serial Status Register (SISTR)	TERR(Transmit Underrun Error)	SH7615 Group SH7616 Group
		RERR(Receive Overrun Error)	
		TDRE(Transmit Data Register Empty)	
		RDRF(Receive Data Register Full)	
SIOF	Serial Status Register (SISTR)	TCD(Transmit Control Data Register Empty)	SH7616 Group
		RCD(Receive Control Data Register Full)	
		TERR(Transmit Underrun Error)	
		RERR(Receive Overrun Error)	

Just when a flag is set to 1, if the flag is read, the read data will be 1, but the internal state will be the same as reading 0.

In that case, if the flag is written 0, the flag is not cleared as 0, because the internal state is the same as reading 0.

[Workaround for Notice 0]

In the case of using a flag of SIO and SIOF, to clear the flag bit certainly, please write it as following sequence.

- 1) Write 0 to the flag after reading 1.
- 2) Then read the flag. If the flag is still read as 1, write 0 to the flag again.

If an interrupt is generated by the flag and the flag causing the interrupt is read in an interrupt handler routine, this case does not apply to the notice 2. However if there is a possibility that another flag bit in the register is set at the timing of reading the register, please follow the workaround described above for another flag bit.

- End of report -