To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A617A/E	Rev.	1.00
Title	Notice about error occurrence in case that one or more DMAC channels are set that transfer request source is external request signal DREQ, or one or more DMAC channels are set that transfer request source is on-chip peripheral module request or auto-request mode and use DACKn pin or TENDn pin.		Information Category	Technical Notification		
Applicable Product	R5S72630P200FP R5S72631P200FP R5S72632P200FP R5S72633P200FP R5S72030W200FP	Lot No. ALL	Reference Document	・SH7263 Group Hardware Manual Rev.1.00 (REJ09B0290-0100) ・SH7203 Group Hardware Manual Rev.1.00 (REJ09B0313-0100)		

Following error occurs in above applicable products of SH2A.

1. Error occurrence conditions and error phenomenon

1) [Condition]

Multiple DMAC channels are used and are in operation. And Among those channels,

- More than 1 channel sets that transfer request source is external request signal DREQ,
- More than 1 are set to burst mode,
- Above 2 conditions are fulfilled and one of below 3 condition is fullfilled
  - ① Channel priority set to round-robin mode
  - ② More than 1 channel of DMAC are set to single address mode
  - ③ More than 1 channel of DMAC are set that transfer source is set to internal address spaces and transfer destination is set to external address spaces.

[Phenomenon]

There is a possibility that DACKn pin and TENDn pin show wrong transfer channel and since then until power-on reset DMA transfer is unavailable. Additionally if this state occurs in burst-mode, CPU becomes unable to fetch instructions, then system becomes suspended.

2) [Condition]

Multiple DMAC channels are used and are in operation. And Among those channels,

- More than 1 channel of DMAC channels are set that transfer request source is on-chip peripheral module request or auto-request mode
- More than 1 are set to burst mode,
- More than 1 channel of DMAC uses DACKn signals or TENDn signals
- Above 3 conditions are fulfilled and one of below 3 condition is fulfilled
  - ① Channel priority set to round-robin mode
  - ② More than 1 channel of DMAC are set to single address mode
  - ③ More than 1 channel of DMAC are set that transfer source is set to internal address spaces and transfer destination is set to external address spaces.

[Phenomenon]

There is a possibility that DACKn pin and TENDn pin show wrong transfer channel.

2. Workarounds

1) In case that one or more DMAC channels are set that transfer request source is external request signal DREQ, please use one of the following four ways.

1-1) Please set all DMAC channels to cycle-steal mode.

1-2) Please set all DMAC channels to burst-mode with all of the following three conditions.

1-2-1) Please set channel priority mode to fixed mode 1 or fixed mode 2.

1-2-2) Please set all DMAC channels to dual-address mode.

1-2-3) Please set transfer source address and transfer destination address of each DMAC channels to one of the followings.

A. transfer source address: external address space transfer destination address: external address space

B. transfer source address: external address space transfer destination address: internal address space

C: transfer source address: internal address space transfer destination address: internal address space

1-3) If there are both of one or more DMAC channels set to cycle-steal mode and one or more DMAC channels set to burst mode, please use with all of the following three conditions.

1-3-1) Please set channel priority mode to fixed mode 1 or fixed mode 2.

1-3-2) Please set all DMAC channels to dual-address mode.

1-3-3) Please set transfer source address and transfer destination address of each DMAC channels to one of the followings.

A. transfer source address: external address space transfer destination address: external address space

B. transfer source address: external address space transfer destination address: internal address space

C: transfer source address: internal address space transfer destination address: internal address space

1-4) Please use only one DMAC channel.

2) In case that one or more DMAC channels are set that transfer request source is on-chip peripheral module request or auto-request mode and use DACKn pin or TENDn pin, please use one of the following four ways.

2-1) Please set all DMAC channels to cycle-steal mode.

2-2) Please set all DMAC channels to burst-mode with all of the following three conditions.

2-2-1) Please set channel priority mode to fixed mode 1 or fixed mode 2.

2-2-2) Please set all DMAC channels to dual-address mode.

2-2-3) Please set transfer source address and transfer destination address of each DMAC channels to one of the followings.

A. transfer source address: external address space transfer destination address: external address space

B. transfer source address: external address space transfer destination address: internal address space

C: transfer source address: internal address space transfer destination address: internal address space

2-3) If there are both of one or more DMAC channels set to cycle-steal mode and one or more DMAC channels set to burst mode, please use with all of the following three conditions.

2-3-1) Please set channel priority mode to fixed mode 1 or fixed mode 2.

2-3-2) Please set all DMAC channels to dual-address mode.

2-3-3) Please set transfer source address and transfer destination address of each DMAC channels to one of the followings.

A. transfer source address: external address space transfer destination address: external address space

B. transfer source address: external address space transfer destination address: internal address space

C: transfer source address: internal address space transfer destination address: internal address space

2-4) Please use only one DMAC channel.

We appreciate your understanding.