Date: Nov. 25, 2013

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A039A/E	Rev.	1.00
Title	Notes When Using A/D Converter Correction and Supplement Information on the INT Interrupt		Information Category	Technical Notification		
Applicable Products	R8C/34K, R8C/34U Groups, R8C/3MK, R8C/3MU Groups	Lot No. –	Reference Document			

1. Notes when using the A/D converter

Applicable products:

R8C/34K Group, R8C/34U Group, R8C/3MK Group, R8C/3MU Group

Phenomenon:

In repeat mode 0, repeat mode 1, or repeat sweep mode, when reading the A/D register i (ADi, i = 0 to 7) while the register value is rewritten, an undefined value may be read. The period for reading an undefined value is one cycle of φAD.

Countermeasure:

Read A/D register i several times in a row to determine whether the read value is valid, or use the A/D converter in one-shot mode or single sweep mode.

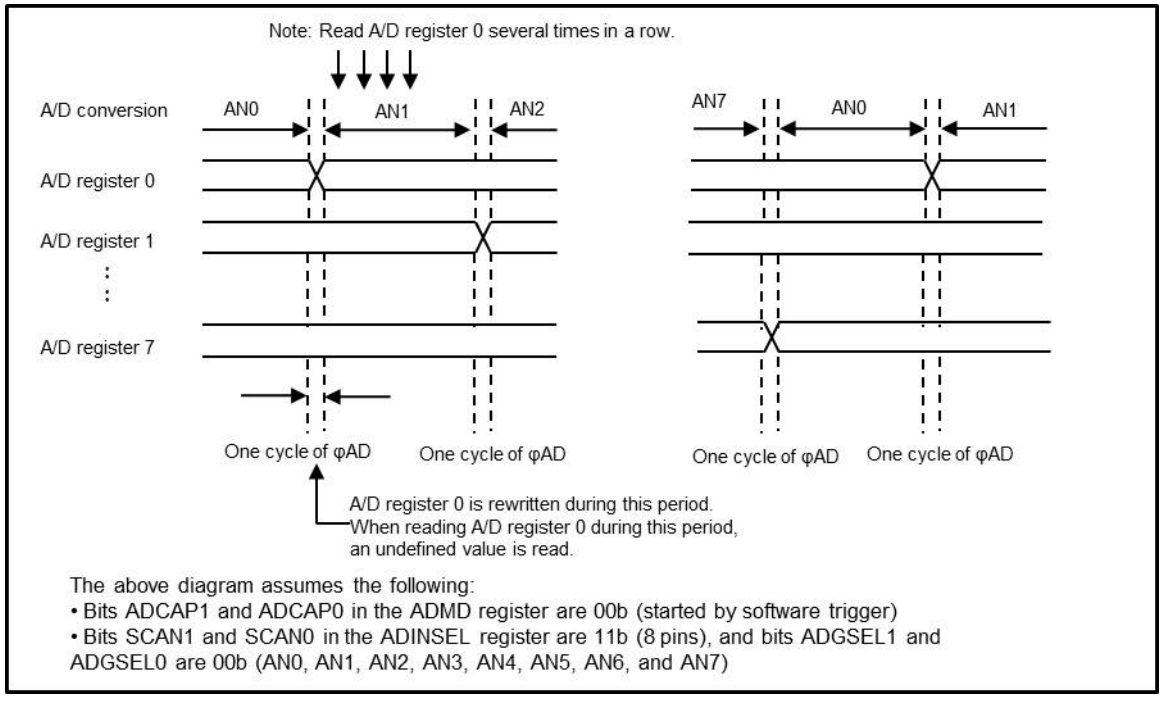

Figure 1 Period When A/D Register i is Rewritten

2. Correction and supplement information on the INT interrupt

Applicable products:

R8C/34K Group, R8C/34U Group

This section corrects and supplements descriptions of registers INTEN and INTF in the R8C/34U Group, R8C/34K Group User's Manual: Hardware Rev.1.00.

11.4.3 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	—	—	INT1PL	INT1EN	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	INT1EN	INT1 input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{INT1}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	INT3EN	$\overline{INT3}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{INT3}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 1 or 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

b0	INT0EN	$\overline{INT0}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{INT0}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

b4	INT2EN	$\overline{INT2}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{INT2}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

11.4.5 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	—	—	INT1F1	INT1F0	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	INT1F0	$\overline{INT1}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	INT3F0	$\overline{INT3}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

b0	INT0F0	$\overline{INT0}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W

b4	INT2F0	$\overline{INT2}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W