To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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(Note) Each URL in the body was changed in each described order as follows.
http://tool-support.renesas.com/jpn/toolnews/sh4_trap/umachine_v5.zip
http://tool-support.renesas.com/jpn/toolnews/sh4_trap/umachine_v6.zip
http://tool-support.renesas.com/jpn/toolnews/sh4_trap/umachine_v7.zip
(When using Ver.8 or later, please modify umachine.h and smachine.h in the same way as the files in umachine_v7.zip)
http://tool-support.renesas.com/jpn/toolnews/sh4_trap/itron.zip

date: 2003/01/22

HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	Microprocessor		No	TN-SH7-456A/E	Rev	1
THEME	The notes on use of TRAPA instruction / SLEEP instruction / Undefined instruction(H'FFFD)	Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	SH7750 SH7750S SH7750R SH7751 SH7751R SH-4 core use product	Lot No. All lots	Reference Documents	SH7750 series hardware manual SH7751 series hardware manual	Effective Date Eternal	

1. Summary

(1) There is a possibility of writing the erroneous data in cache when TRAPA instruction or Undefined instruction code H'FFFD is executed.

(2) When TRAPA instruction or Undefined instruction code H'FFFD is executed, the ITLB hit judgment may be mistaken. Then, after re-registration, there is a possibility to generate the ITLB multi-hit exception.

(3) There is a possibility of writing the erroneous data in the FPU registers or MACH and MACL registers, when TRAPA instruction or SLEEP instruction or Undefined instruction code H'FFFD is executed.

2. Generated condition

2.1 There is a possibility of writing a wrong instruction to Instruction cache when three following conditions consist at the same time.

1) Instruction cache is ON. (CCR.ICE=1)
2) TRAPA instruction or Undefined instruction code H'FFFD in a Cache On Space (U0/P0/P1/P3 space) is executed.
3) The code interpreted as the instruction (both read and write) accessed to the address (0xF0000000 - 0xF7FFFFFF) exists in following 4 words of TRAPA instruction or Undefined instruction code H'FFFD of above-mentioned 2).

2.2 There is a possibility of writing the erroneous data in Operand cache when three following conditions consist at the same time.

1) Operand cache is ON.(CCR.OCE=1)
2) Undefined instruction code H'FFFD is executed.
3) The code interpreted as the OCBI/OCBP/OCBWB/TAS.B instruction accessed to the built-in store queues address (0xE0000000 -0xE3FFFFFF) exists in following 4 words of Undefined instruction code H'FFFD of above-mentioned 2).

2.3 There is a possibility to which the ITLB hit judgment is mistaken when three conditions of the following conditions consist at the same time. When the ITLB hit is mistaken and it is judged that it makes a mistake, re-registration to ITLB is done. After that, there is a possibility to generate the ITLB multi-hit exception.

1) MMU is ON. (MMUCR.AT=1)

2) TRAPA instruction or Undefined instruction code H'FFFD in the TLB conversion space (U0 / P0 / P3 space) is executed.

3) The code interpreted as the instruction (both read and write) accessed to the address (0xF0000000 – 0xF7FFFFFF) exists in following 4 words of TRAPA instruction or Undefined instruction code H'FFFD of above-mentioned 2).

2.4 There is a possibility of writing a wrong value to register (FR0-FR15,XF0-XF15,FPSCR,and FPUL) related to FPU, MACH, and MACL when two following conditions consist at the same time.

1) TRAPA or SLEEP instruction or Undefined instruction code H'FFFD is executed.

2) The code interpreted in combining FPSCR and PR at that time in following 8 words of TRAPA or SLEEP instruction or Undefined instruction code H'FFFD of above-mentioned 1), excluding H 'FFFD in H'Fxxx (the instruction whose initial 4 bits are H’F) as an Undefined instruction exists.

Example : Instruction H'FxxE (x: arbitrary hexadecimal number) is defined here as an Undefined instruction in FPSCR.PR=1.

[Note]For the number of following instructions, internally, there is a possibility that this trouble occurs in case of 2.1-2.3 is following 2xI clock, and in case of 2.4 is the case of it is executable within following 4xI clock . Therefore, the number of instructions which can be executed in 2xI clock or 4xI clock is maximum 4 instructions or maximum 8 instructions respectively.

3. Workaround

3.1 Please take measures of either following (1) or (2).

(1) Please put the NOP instruction on eight following words of TRAPA instruction, SLEEP instruction, and Undefined instruction code H'FFFD.

(2) Please put “OR R0,R0” instruction on five following words of TRAPA instruction, SLEEP instruction, and Undefined instruction code H'FFFD. The OR instruction is not executed simultaneously. Therefore, because it requires more than 5xI clock for execution, “In case of H'Fxxx exists in eight following words" of the generation condition of 2.4(2) can be evaded.

3.2 Workaround when compiler is used

3.2.1 In case of using built-in function sleep and trapa

(1) Smachine.h and umachine.h files in compiler system directory are backed up.

PC version: (1) In case of HEW system

"HEW Installation directory "¥Tools¥Hitachi¥Sh¥"Version"¥include

(2) In case of HIM system

"HIM Installation directory" ¥Toolchains¥Hitachi¥Shc¥"Version"¥include

In case of UNIX system

"Compiler system installation directory"

(2) smachine.h and umachine.h are downloaded from the following, and they are copied onto the place of (1).

URL:

(V5)

http://www.hitachisemiconductor.com/sic/jsp/japan/jpn/PRODUCTS/MPUMCU/TOOL/download/crosstool/release/sh4_trap/umachine_v5.zip

(V6)

http://www.hitachisemiconductor.com/sic/jsp/japan/jpn/PRODUCTS/MPUMCU/TOOL/download/crosstool/release/sh4_trap/umachine_v6.zip

(V7)

http://www.hitachisemiconductor.com/sic/jsp/japan/jpn/PRODUCTS/MPUMCU/TOOL/download/crosstool/release/sh4_trap/umachine_v7.zip

(3) The assembler file output specification is done for the file which uses sleep and trapa built-in function.
Moreover, trapa built-in function is also used in HI7750, but regarding HI7750, please refer to 3.3.

3.2.2 Please use either of the following methods when you use built-in function trapa_svc.

Method 1:

(1) The assembly file output specification is done for the file which uses trapa_svc built-in function.

(2) Please add “five or instructions” and “one nop instruction” to the immediately after the trapa instruction of the output assembly source.

Example:

Before change (ASM source)

```
:
MOV.L L236+2,R0  ; H'0000FFC8
MOV   #5,R4
TRAPA #63
:
:
```

After change (ASM source)

```
:
   MOV.L L236+2,R0  ; H'0000FFC8
MOV   #5,R4
TRAPA #63
OR    R0,R0
OR    R0,R0
OR    R0,R0
OR    R0,R0
OR    R0,R0
NOP
```

[Note]The following error messages might come out by the assembly source after it changes.

"File name"("Line - number") 402 (E) ILLEGAL VALUE IN OPERAND

Please use method 2 when this error is output.

Method 2:

(1) The in-line assembler function which outputs the or instruction is added, and calls it just behind the trapa_svc built-in function.

Example :

```
#pragma inline_asm(OR(size=12))          /* Addition */
    static void OR( ){          /* Addition : Five OR Instruction and one NOP Instruction are described.  */
                or   r0,r0
                or   r0,r0
                or   r0,r0
                or   r0,r0
                or   r0,r0
                nop
        }
        void func( ){
                :
                trapa_svc(63,0x8,0x5);
                OR( );                          /* Addition */
                :
        }
```

(2) The assembly file output specification is done for the file which uses trapa_svc built-in function.

(3) Please confirm the output assembly program. And please confirm or instructions 5 pieces are output just behind the trapa instruction. When BRA + literal data line is generated between trapa instruction and or instruction line, trapa instruction is moved just before or, please deletes nop immediately after or instruction line.

Example:

Before change (ASM source)

```
        TRAPA     #63
        BRA       L238
        NOP
L239:
        .RES.W    1
        .DATA.L   H'0000FF80
L238:
        or   r0,r0
        or   r0,r0
        or   r0,r0
        or   r0,r0
        nop
```

After change (ASM source)

```
        NOP                ; Change
        BRA       L238
        NOP
L239:
        .RES.W    1
        .DATA.L   H'0000FF80
L238:
TRAPA     #63      ; Change
or   r0,r0
or   r0,r0
or   r0,r0
or   r0,r0
or   r0,r0
```

Moreover, trapa_svc built-in function is also used in HI7750, but regarding HI7750, please refer to 3.3.

3.2.3 When you use trap instruction return specification (tn=) as an interrupt specification of # pragma interrupt specification function, please use either of the following methods.

Method 1 :

(1) The assembly file output specification is done for the file which uses the trap instruction return specification.

(2) Please add “five or instructions” and “one nop instruction” to the immediately after the trapa instruction.

Example:

Before change (ASM source)	After change (ASM source)
:	:
TRAPA #0	TRAPA #0
:	OR R0,R0
:	OR R0,R0
	OR R0,R0
	OR R0,R0
	OR R0,R0
	NOP

[Note]The following error messages might come out by the assembly source after it changes.

"File name"("Line - number") 402 (E) ILLEGAL VALUE IN OPERAND

Please use method 2 when this error is output.

Method 2:

(1) The in-line assembler function which outputs the or instruction is added, and calls it by the end of the trap instruction return specification function.

Example:

```
#pragma interrupt (func(tn=63))
#pragma inline_asm(or, (size =12))   /*Addition */
static void OR( ){                          /* Addition : Five OR instructions are described.  */
        or    r0,r0
        or    r0,r0
        or    r0,r0
        or    r0,r0
        or    r0,r0
}
void func( ){
        :
        OR( );                              /* Addition */
}
```

(2) The assembly file output specification is done for the file which uses the trap instruction return specification.

(3) In the output assembly program, please move the or instruction line immediately after trapa instruction.

Example:

Before change (ASM source)

```
or    r0,r0
or    r0,r0
or    r0,r0
or    r0,r0
or    r0,r0
.ALIGN    4
FMOV.S    @R15+,FR0
FMOV.S    @R15+,FR1
FMOV.S    @R15+,FR2
FMOV.S    @R15+,FR3
FMOV.S    @R15+,FR4
FMOV.S    @R15+,FR5
FMOV.S    @R15+,FR6
FMOV.S    @R15+,FR7
FMOV.S    @R15+,FR8
FMOV.S    @R15+,FR9
FMOV.S    @R15+,FR10
FMOV.S    @R15+,FR11
MOV.L     @R15+,R0
MOV.L     @R15+,R1
MOV.L     @R15+,R2
MOV.L     @R15+,R3
MOV.L     @R15+,R4
MOV.L     @R15+,R5
MOV.L     @R15+,R6
MOV.L     @R15+,R7
TRAPA     #63
```

After change (ASM source)

```
; Deletion
; Deletion
; Deletion
; Deletion
; Deletion
; Deletion
FMOV.S    @R15+,FR0
FMOV.S    @R15+,FR1
FMOV.S    @R15+,FR2
FMOV.S    @R15+,FR3
FMOV.S    @R15+,FR4
FMOV.S    @R15+,FR5
FMOV.S    @R15+,FR6
FMOV.S    @R15+,FR7
FMOV.S    @R15+,FR8
FMOV.S    @R15+,FR9
FMOV.S    @R15+,FR10
FMOV.S    @R15+,FR11
MOV.L     @R15+,R0
MOV.L     @R15+,R1
MOV.L     @R15+,R2
MOV.L     @R15+,R3
MOV.L     @R15+,R4
MOV.L     @R15+,R5
MOV.L     @R15+,R6
MOV.L     @R15+,R7
TRAPA     #63
or    r0,r0          ; Addition
or    r0,r0          ; Addition
or    r0,r0          ; Addition
or    r0,r0          ; Addition
or    r0,r0          ; Addition
.ALIGN    4          ; Addition
```

3.3 Workaround when HI series OS is used

Though there are the following three products in HI series OS for SH-4, counter measures are necessary only for using HI7750.

However, when you use TRAPA instruction, SLEEP instruction, and Undefined instruction code H'FFFD by the application, please take measures of 3.1 and 3.2 regardless of OS.

(1)HI7750 (ìITRON3.0 Specification conforming)

(2)HI7750S/3 (ìITRON3.0 Specification conforming)

(3)HI7750/4 (ìITRON4.0 Specification conforming)

SLEEP instruction and Undefined instruction code H'FFFD is not used though the TRAPA instruction is used in HI7750.

3.3.1 Issue of HI7750 system call

(1) In case of issuing the System call by Assembly language

Please take measure of 3.1.

(2) In case of issuing the System call by C language

It was a mechanism that the system call is called by trapa() and trapa_svc() of the built-in function of C compiler in HI7750. However, we will take measure not to use trapa() and trapa_svc().

(a) Please download the following files, and defrost to an arbitrary directory.

The following files are generated when defrosting, and copy it onto a specified place respectively, please.

Moreover, No.1 to No.3 become the correction version of an existing file.

Please backup it beforehand if it is necessary.

No.	File name	Directory at copy area
1	itron.h	hihead
2	hish7.h	hihead
3	hish77.h	hihead
4	trap_cif.src	Arbitrary directory such as hiuser

Download URL :

http://www.hitachisemiconductor.com/sic/jsp/japan/jpn/PRODUCTS/MPUMCU/TOOL/download/crosstool/release/sh4_trap/itron.zip

(b) Please compile all application file of the C language description again.

(b) Please assemble and link files of above-mentioned No.4 when you generate the load module of the absolute address form.

3.3.2 TRAPA instruction in HI7750

In the object initial registration part in Kernel build file (hibuild.usr) and Setup file (hisetup.usr), in case of using following initial macro, and when the mistake is found in the specified initial registered information, it originally becomes a system down.

However, in the order of the linkage, in this case, there is a possibility of corresponding to the trouble generation condition which has been described to 3) in clause 2.

• _INI_VCRE_TSK

• _INI_VSCR_TSK

Moreover, it is similar when the mistake is found in the I/O handler initial registration part.

To evade this trouble, please do not mistake for these setting.

3.3.3 Type name and version of HI7750

Type name: HS0775ITCE1SME, HS0775ITCE1SMB, HS0775ITCE1SMS, HS0775ITHE1STE, HS0775ITHE1STB, HS0775ITHE1STS, HS0775ITIE1SFE, HS0775ITIE1SFB, HS0775ITIE1SFS, HS0775ITIE1SFE-E, HS0775ITIE1SFB-E, HS0775ITIE1SFS-E, HS0775ITIE1SFU, HS0775ITIE1SFV, HS0775ITIE1SFW, HS0775ITIE1SFX, HS0775ITIE1SFY, HS0775ITIE1SFZ

Version: All versions