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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-SH7-A896A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Notes on Usage of the DTC for IIC2 and IIC3 | | Information Category | Technical Notification | | |
| Applicable Product | See below. | Lot No.<br>All lots | Reference Document | See below. | | |

This update concerns usage of the $I^2C$ bus interface 2 (IIC2) and $I^2C$ bus interface 3 (IIC3) in the products listed below.

[Precaution]

**1. DTC Transfers Using the IIRXI Interrupt as the Source**

If the handler of the IIRXI interrupt generated after a DTC transfer clears RDRF in ICSR to 0 or reads ICDRR, it may not be possible to receive the next data.

As a workaround for this issue, perform both 1 and 2 below:

1. For DTC transfers that use the IIRXI interrupt as the source, clear to 0 the DISEL bit in the DTC's MRB register.
2. The processing routine for the IIRXI interrupt must clear the RDRF flag in ICSR by the time of the rising edge of the ninth clock cycle of the next frame to be transferred.

**2. DTC Transfers Using the IITXI Interrupt as the Source**

If the handler of the IITXI interrupt generated after a DTC transfer clears TDRE in ICSR to 0, unintended data transmission may occur. Also, writing transmit data to ICDRT may disrupt transmission of the last data transferred by the DTC.

As a workaround for this issue, perform all of 1 to 4 below:

1. For DTC transfers that use the IITXI interrupt as the source, clear to 0 the DISEL bit in the DTC's MRB register.
2. In transmit mode (TRS = 1), do not access ICSR to clear TDRE to 0.
3. Ensure that the IITXI interrupt handler clears TIE in ICIER to 0 to disable the IITXI interrupt. After TIE is cleared, read ICIER before ending handling of the IITXI interrupt.
4. When writing transmit data to ICDRT after a DTC transfer finishes, make sure to set TEND to 1 before writing to ICDRT. (After TEND is set to 1, enable DTC transfers using the IITXI interrupt as the source.)

[Correction of Errors in the User's Manuals]

Taking the *SH7214 Group, SH7216 Group User's Manual: Hardware* as an example, we would like to inform you of the correction of errors in the User's Manuals.

**8.2.2 DTC Mode Register B (MRB)**

**[Before correction (p.211)]**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| | | | | |
| 5 | DISEL | Undefined | — | DTC Interrupt Select<br>When this bit is set to 1, an interrupt request is generated to the CPU every time a data transfer or a block transfer ends. When this bit is set to 0, a CPU interrupt request is only generated when the specified number of data transfers ends. |
| | | | | |

**[After correction]**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| | | | | |
| 5 | DISEL | Undefined | — | DTC Interrupt Select<br>When this bit is set to 1, an interrupt request is generated to the CPU every time a data transfer or a block transfer ends. When this bit is set to 0, a CPU interrupt request is only generated when the specified number of data transfers ends.<br>Note: Set this bit to 0 when the IIC3 is selected as the activation source. |
| | | | | |

**[Addition (p.1029)]**

**19.8.10. DTC Transfers Using the IIRXI Interrupt as the Source**

If the handler of the IIRXI interrupt generated after a DTC transfer clears RDRF in ICSR to 0 or reads ICDRR, it may not be possible to receive the next data.

As a workaround for this issue, perform both 1 and 2 below:

1. For DTC transfers that use the IIRXI interrupt as the source, clear to 0 the DISEL bit in the DTC's MRB register.
2. The processing routine for the IIRXI interrupt must clear the RDRF flag in ICSR by the time of the rising edge of the ninth clock cycle of the next frame to be transferred.

**19.8.11. DTC Transfers Using the IITXI Interrupt as the Source**

If the handler of the IITXI interrupt generated after a DTC transfer clears TDRE in ICSR to 0, unintended data transmission may occur. Also, writing transmit data to ICDRT may disrupt transmission of the last data transferred by the DTC.

As a workaround for this issue, perform all of 1 to 4 below:

1. For DTC transfers that use the IITXI interrupt as the source, clear to 0 the DISEL bit in the DTC's MRB register.
2. In transmit mode (TRS = 1), do not access ICSR to clear TDRE to 0.
3. Ensure that the IITXI interrupt handler clears TIE in ICIER to 0 to disable the IITXI interrupt. After TIE is cleared, read ICIER before ending handling of the IITXI interrupt.

4. When writing transmit data to ICDRT after a DTC transfer finishes, make sure to set TEND to 1 before writing to ICDRT. (After TEND is set to 1, enable DTC transfers using the IITXI interrupt as the source.)

**[Applicable Products and Related Documents]**

| Family | Group | Related Documents | Rev. | Control Code |
|---|---|---|---|---|
| **SH7080** | SH7084, SH7085, SH7086 | SH7080 Group User's Manual: Hardware | 5.00 | R01UH0198EJ0500 |
| **SH7137** | SH7131, SH7132, SH7136, SH7137 | SH7137 Group Hardware Manual | 3.00 | REJ09B0402-0300 |
| **SH7216** | SH7214, SH7216 | SH7214 Group, SH7216 Group User's Manual: Hardware | 4.00 | R01UH0230EJ0400 |
| **SH7231** | SH7231 | SH7231 Group User's Manual: Hardware | 2.00 | R01UH0073EJ0200 |
| **SH7280** | SH7285, SH7286 | SH7280 Group, SH7243 Group User's Manual: Hardware | 3.00 | R01UH0229EJ0300 |