To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)
Send any inquiries to http://www.renesas.com/inquiry.
We would like to inform you of our notes on TRS bit setting and ICDR register access in the I²C bus interface of H8/300H Tiny series and H8S series. When reading the ICDR register in Transmit mode (TRS = 1) or when writing to the ICDR register in receive mode (TRS = 0), the clock could be outputted to SCL bus line under certain conditions. This happens because the low-fixation of the SCL pins will be cancelled before the regular ICDR register access. Please read the following paragraphs carefully.

1. Applicable function

I²C bus interface module

2. Conditions to cause this failure.

Low-fixation of the SCL pins is cancelled incorrectly when the following conditions are satisfied.

2-1. Master mode

Figure 1 shows the notes on ICDR reading (TRS = 1) in master mode.

Low-fixation of the SCL pins are also cancelled incorrectly when all of the following conditions are satisfied.

(1) When previously received 2-bytes data remains in ICDR unread (ICDRS are full).
(2) Reads ICDR register after switching to transmit mode (TRS=1). (RDRF=0 state)
(3) Sets to receive mode (TRS =0), after transmitting Rev.1 frame of issued start condition by master mode.

2-2. Slave mode

Figure 2 shows the notes on ICDR writing (TRS = 0) in slave mode.

(1) Writes ICDR register in receive mode (TRS = 0), after entering the start condition by slave mode (TDRE=0 state).

Address match with Rev.1 frame, receive 1 by R/W bit, and switches to transmit mode (TRS = 1).

When these conditions are satisfied, the low fixtion of the SCL pins is cancelled without ICDR register access after Rev.1 frame is transferred.

3. Restriction

Please carry out the following countermeasures when transmitting/receiving via the IIC bus interface module.

(1) Please read the ICDR registers in receive mode, and write them in transmit mode.
(2) In receiving operation with master mode, please issue the start condition after clearing the internal flag of the IIC bus interface module, using CLR3-0 bit of the DDCSWR register on bus-free state (BBSY = 0).
Figure 1. Notes on ICDR reading with TRS=1 setting in master mode.

Figure 2. Notes on ICDR writing with TRS=0 setting in slave mode.