To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU/MCU		Document No.	TN-R8C-A006A/E	Rev.	1.00
Title	Notes on Timer RG		Information Category	Technical Notification		
Applicable Product	R8C/36A Group, R8C/38A Group, R8C/Lx Series	Lot No.	Reference Document			

Please note the following when using timer RG for the above applicable products.

1. Notes on timer RG

(1) When writing to the TRG register or TRGCR register, make sure the TSTART bit in the TRGMR register to 0 (count stops).

(2) When setting bits IMFA, IMFB, UDF, or OVF in the TRGSR register to 0, use the MOV instruction to ensure that only the specified bits are written to 0 and the other bits are written to 1. Write 0Fh to this register immediately after writing to these bits. Do not generate an interrupt or a DTC transfer until 0Fh is written.

(3) When reading the TRGSR register after writing to it, insert one or more NOP instructions between the instructions used for writing and reading.

(4) When using the output compare function in timer mode, use the TRGIOR register to select the compare match output from the following three: low-level output, high-level output, or toggle output. When waveform output mode is selected, the port functions as the compare match output pin (TRGIOA or TRGIOB) while the TRGIOASEL bit or the TRGIOBSEL bit in the TIMSR register (1) is 1. The output level of these pins depend on the settings of bits IOA0 and IOA1, or bits IOB0 and IOB1 in the TRGIOR register until the first compare match occurs.

After setting the TRGIOR register, the output level is undefined for one cycle of the timer RG operating clock, and the corresponding level to bits IOA0 and IOA1 or bits IOB0 and IOB1 is output.

Note:

1. These bits apply to the R8C/36A Group and R8C/38A Group. In the R8C/Lx Series, this condition applies to the TRGIOASEL0 bit or the TRGIOBSEL0 bit in the TRGPSR register.

(5) When using PWM mode, the TRGIOA pin becomes the PWM output pin by setting the PWM bit in the TRGMR register to 1 (PWM mode) while the TRGIOASEL bit in the TIMSR register (1) is 1. The output level of the PWM output pin depends on the settings of bits CCLR0 and CCLR1 in the TRGCR register until the first compare match occurs.

After setting the PWM bit, the output level is undefined for one cycle of the timer RG operating clock, and the corresponding level to bits CCLR0 and CCLR1 is output.

Note:

1. This bit applies to the R8C/36A Group and R8C/38A Group. In the R8C/Lx Series, this condition applies to the TRGIOASEL0 bit in the TRGPSR register.

2. TIMSR register

Due to an error in the TIMSR register in the R8C/36A Group and R8C/38A Group hardware manuals, refer to the revised register shown below.

- R8C/36A Group hardware manual Rev.0.20 (REJ09B0480-0020)
- R8C/38A Group hardware manual Rev.0.10 (REJ09B0485-0010)

Timer Pin Select Register (TIMSR)

Address 0186h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRGCLKBSEL	TRGCLKASEL	TRGIOBSEL	TRGIOASEL	—	TRFISEL0	—	TREOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TREOSEL0	TREO pin select bit	0: P0_4 pin assigned 1: P6_0 pin assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRFISEL0	TRFI pin select bit	0: TRFI pin not used 1: P8_3 pin assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRGIOASEL	TRGIOA pin select bit	0: TRGIOA pin not used 1: P5_6 pin assigned	R/W
b5	TRGIOBSEL	TRGIOB pin select bit	0: TRGIOB pin not used 1: P5_7 pin assigned	R/W
b6	TRGCLKASEL	TRGCLKA pin select bit	0: TRGCLKA pin not used 1: P3_0 pin assigned	R/W
b7	TRGCLKBSEL	TRGCLKB pin select bit	0: TRGCLKB pin not used 1: P3_2 pin assigned	R/W

The TIMSR register selects which pin is assigned as the timer RG I/O. To use the I/O pin for timer RG, set this register.
Set the TIMSR register before setting the registers associated with timers RE, RF, and RG. Also, do not change the setting value in this register during the operation of timers RE, RF, and RG.