RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A052A/E	Rev.	1.00
Title	Notes on Sub-clock Initialization in the RX630 Group, RX63N Group, and RX631 Group		Information Category	Technical Notification		
Applicable Product	RX630 Group RX63N Group, RX631 Group	Lot No. All	Reference Document	RX630 Group User's Manual: Hardware Rev.1.50 (R01UH0040EJ0150) RX63N Group, RX631 Group User's Manual: Hardware Rev.1.60 (R01UH0041EJ0160)		

1. Notes

Registers associated with the sub-clock include registers whose values are undefined after a reset, and registers that require the sub-clock to be temporarily stopped before being rewritten.
Since the sub-clock starts oscillating at power-on, make sure to carefully follow notes in the corresponding user's manual when setting a value in such registers.
Table 1.1 lists notes on initialization of the sub-clock described in the user's manuals.

Table 1.1 Notes on Sub-Clock Initialization (1/2)

Item	Value after reset	Notes
General	—	• Oscillation of the sub-clock is controlled with both bits SOSCCR.SOSTP and RCR3.RTCEN. • When using the sub-clock as a system clock, control the sub-clock with the SOSCCR.SOSTP bit. • When using the sub-clock as a count source of the realtime clock (RTC), control the sub-clock with the RCR3.RTCEN bit. • When not using the sub-clock, set bits SOSCCR.SOSTP and RCR3.RTCEN to 1 and 0, respectively. • Before oscillating the sub-clock, make sure to also set bits b3 to b1 in the RCR3 register for the RX630 Group (the RCR3.RTCDV[2:0] bits in the RX63N and RX631 Groups).
SOSCCR.SOSTP bit	0	• After modifying this bit, confirm that the bit has been rewritten and then execute the next instruction. • Before setting this bit to 0, make sure to set the SOSCWTCR register. • After setting this bit to 0, make sure that oscillation stabilization wait time has elapsed and then start using the sub-clock. • Before modifying this bit to 0 from 1, make sure to wait for at least five cycles of the sub-clock. • When setting this bit to 1, make sure that oscillation is stable. • When not using the sub-clock, set this bit to 1.
SOSCWTCR.SSTS[4:0] bits	00110b or 00000b	• Set these bits so the total of the wait time and oscillation stabilization wait offset time is equal to or greater than the oscillator stabilization time. • After the sub-clock starts oscillating, make sure that oscillation stabilization wait time has elapsed and then use the sub-clock. • These bits can be modified only when the SOSCCR.SOSTP bit is 1.

Table 1.1 Notes on Sub-Clock Initialization (2/2)

Item	Value after reset	Notes
RCR3.RTCEN bit	Undefined	• The peripheral module clock (PCLK) frequency must be equal to or higher than the count source frequency. • After modifying this bit, read the bit to confirm the value has been updated and then execute the next process. • When the RCR4.RCKSEL bit is 1, oscillation of the sub-clock cannot be controlled with this bit. • If this bit is set to 1, the sub-clock does not stop oscillating even in software standby mode.
Bits b3 to b1 in RCR3 register for the RX630 Group (RCR3.RTCDV[2:0] bits in the RX63N and RX631 Groups)	Undefined	• PCLK frequency must be equal to or higher than the count source frequency. • During oscillation of the sub-clock, do not modify these bits. • After modifying these bits, confirm that the value has been updated and then execute the next process.
RCR4.RCKSEL bit	Undefined	• This bit can be set only once after power-on.

2. Sub-clock Initialization Procedures

The following are examples of how to perform initialization while the system clock is in the state after a reset (i.e., at LOCO clock divided by 1).

A. When using the sub-clock as a count source of the RTC

Since the sub-clock is enabled by setting the RCR3.RTCEN bit to 1 (sub-clock oscillator is running), the sub-clock does not stop even in software standby mode. However, when the SOSCCR.SOSTP bit is 0, since the MCU waits for the number of cycles preset in the SOSCWTCR.SSTS[4:0] bits when exiting software standby mode, it takes time. Therefore, make sure to set the SOSCWTCR.SSTS[4:0] bits again so that the sub-clock oscillator stabilization wait time is minimized.

The sub-clock initialization procedure assuming these conditions is as follows:

(1) Select the RTC count source

The RCR4.RCKSEL bit is undefined at power-on; therefore, select the sub-clock as the RTC count source. Since the sub-clock frequency is lower than LOCO clock frequency, the system clock does not need to be changed.

(2) Stop the sub-clock

Stop the sub-clock temporarily to modify bits b3 to b1 in the RCR3 register for the RX630 Group (the RCR3.RTCDV[2:0] bits in the RX63N and RX631 Groups).

(3) Set bits in the RCR3 register

In the RX630 Group, set bits b3 to b1 to 110b. In the RX63N Group and the RX631 Group, set the RTCDV[2:0] bits to 110b or 001b according to the crystal being used.

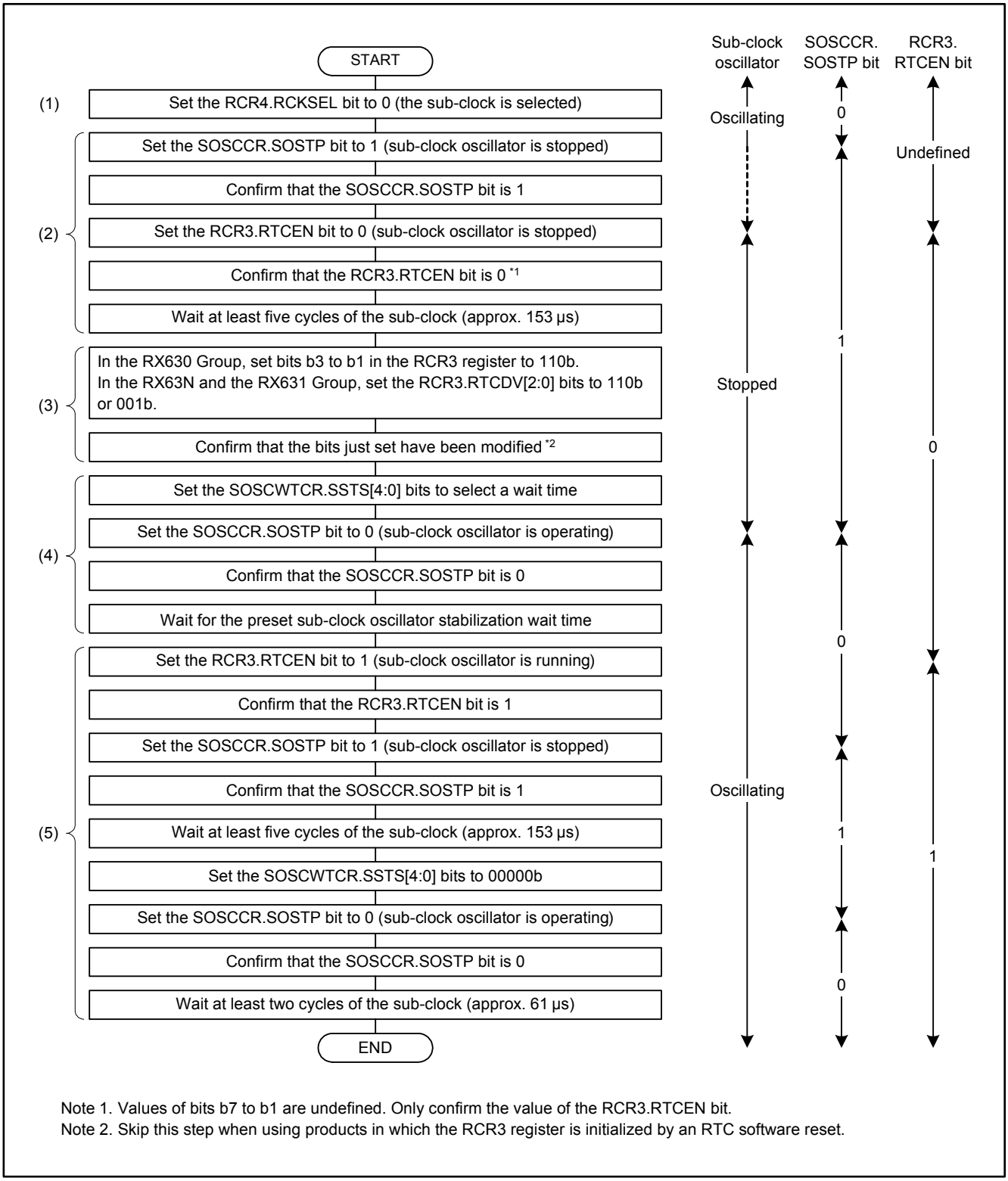
(4) Oscillate the sub-clock

Set wait time of the sub-clock oscillator and then set the SOSCCR.SOSTP bit to 0 (sub-clock oscillator is operating).

(5) Minimize the sub-clock oscillator stabilization wait time

Set the SOSCWTCR.SSTS[4:0] bits to 00000b in order to minimize the time required for exiting software standby mode. To modify the SOSCWTCR register, temporarily set the SOSCCR.SOSTP bit to 1 after setting the RCR3.RTCEN bit to 1 so the sub-clock does not stop oscillating.

Figure 2.1 shows a flowchart of the procedure described above.



Note 1. Values of bits b7 to b1 are undefined. Only confirm the value of the RCR3.RTCEN bit.
Note 2. Skip this step when using products in which the RCR3 register is initialized by an RTC software reset.

Figure 2.1 Initialization Flowchart When Using the Sub-clock as an RTC Count Source

B. When using the sub-clock only as an RTC count source

Unlike the procedure described in the user's manuals, the following is an example of how to oscillate the sub-clock while the SOSCCR.SOSTP bit is 1 (sub-clock oscillator is stopped). Oscillation of the sub-clock is controlled with the RCR3.RTCEN bit. In this case, oscillation of the sub-clock is not influenced by software standby mode.

The sub-clock initialization procedure assuming these conditions is as follows:

(1) Select the RTC count source

The RCR4.RCKSEL bit is undefined at power-on; therefore, select the sub-clock as the RTC count source. Since the sub-clock frequency is lower than the LOCO clock frequency, the system clock does not need to be changed.

(2) Stop the sub-clock

Stop the sub-clock temporarily to modify bits b3 to b1 in the RCR3 register for the RX630 Group (the RCR3.RTCDV[2:0] bits in the RX63N and RX631 Groups).

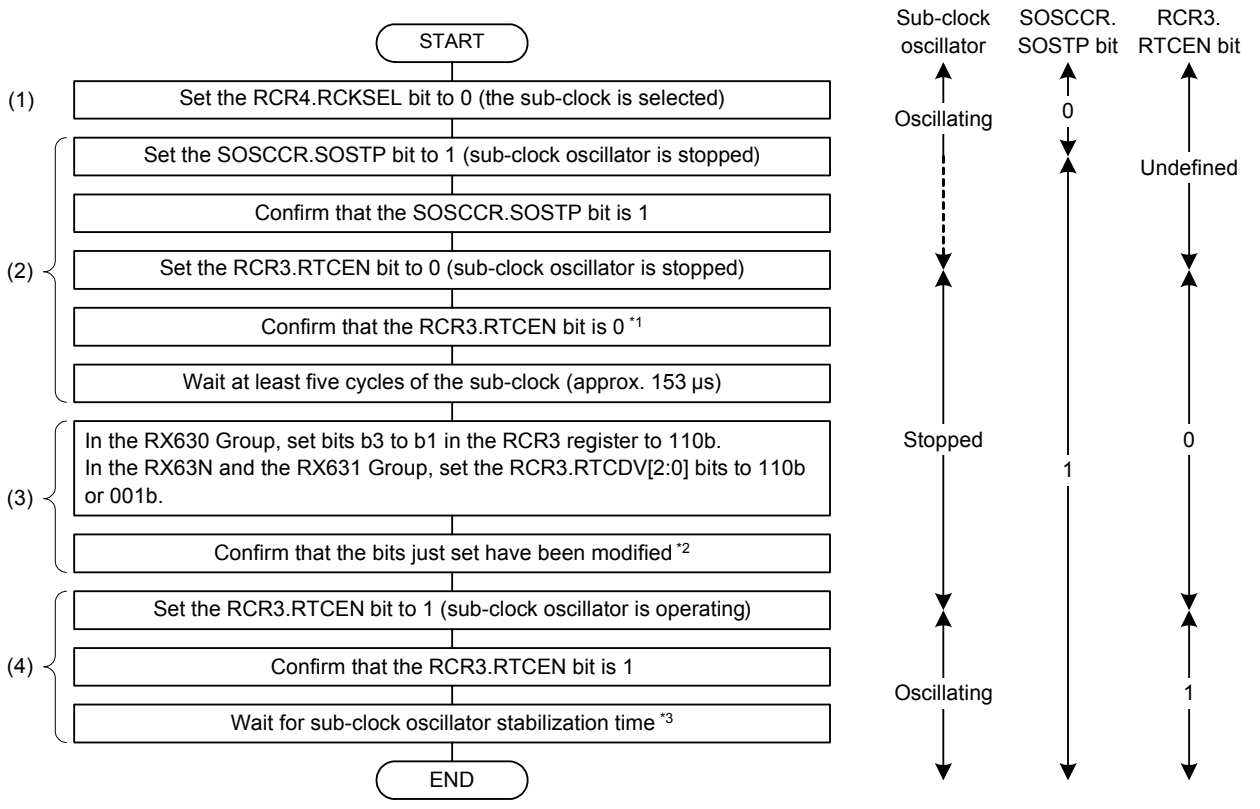
(3) Set bits in the RCR3 register

In the RX630 Group, set bits b3 to b1 to 110b. In the RX63N Group and the RX631 Group, set the RTCDV[2:0] bits to 110b or 001b according to the crystal being used.

(4) Oscillate the sub-clock

Set the RCR3.RTCEN bit to 1 to oscillate the sub-clock.

Figure 2.2 shows a flowchart of the procedure described above.



Note 1. Values of bits b7 to b1 are undefined. Only confirm the value of the RCR3.RTCEN bit.
Note 2. Skip this step when using products in which the RCR3 register is initialized by an RTC software reset.
Note 3. When using products in which the RCR3 register is initialized by an RTC software reset, wait for t_{SUBOSC}. Otherwise wait for t_{SUBOSC} or $t_{SUBOSCWT0}$, whichever is greater.

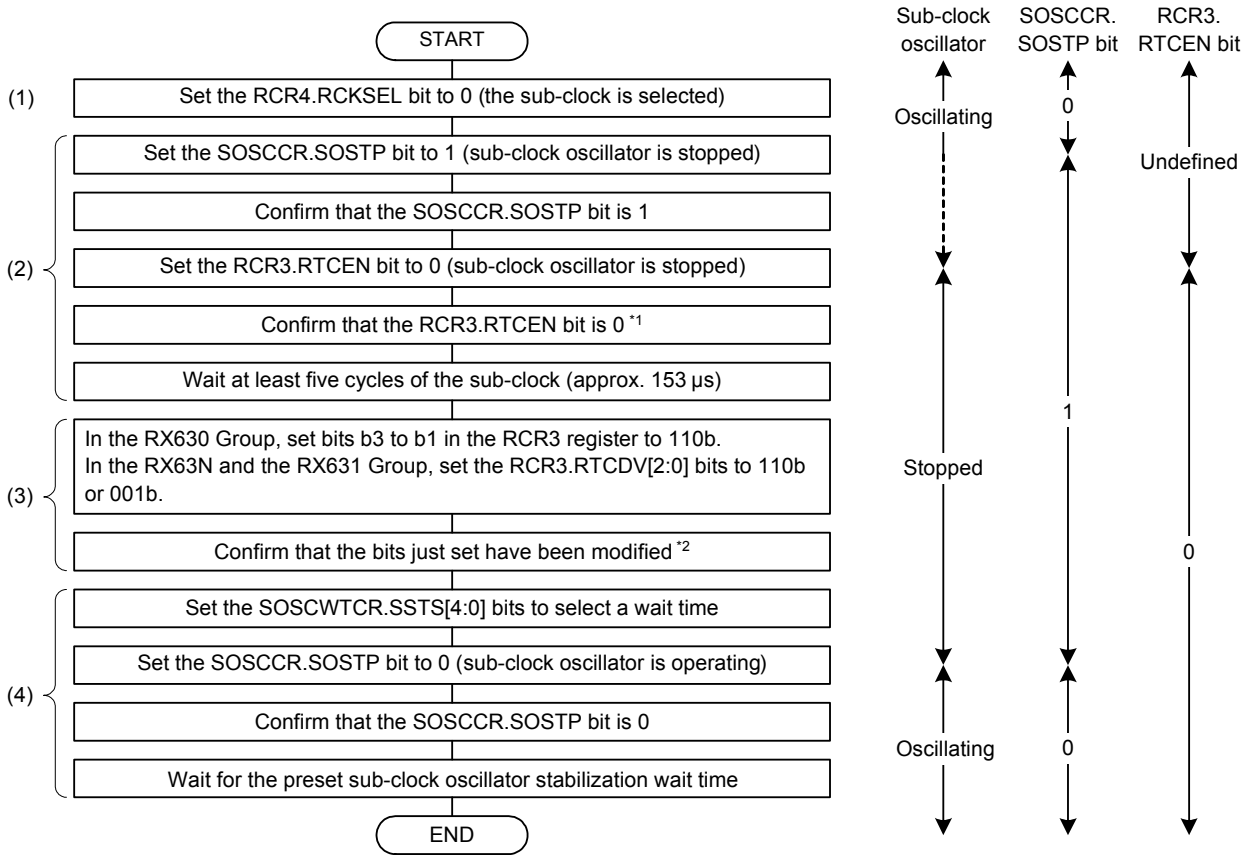
Figure 2.2 Initialization Flowchart When Using the Sub-clock Only as an RTC Count Source

C. When using the sub-clock only as a system clock

Since the RCR3.RTCEN bit is set to 0 (sub-clock oscillator is stopped), the sub-clock stops in software standby mode.

The sub-clock initialization procedure assuming this condition is identical to steps (1) to (4) described in A. “When using the sub-clock as a count source of the RTC”.

Figure 2.3 shows a flowchart of the procedure described above.



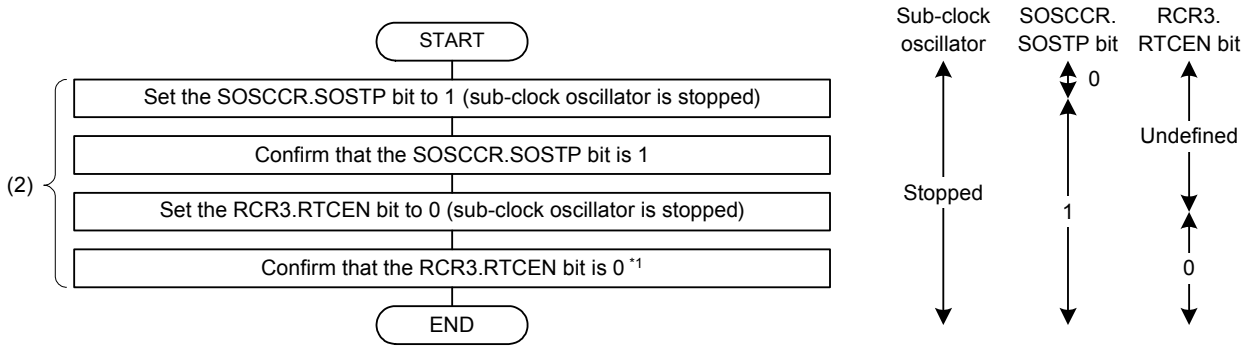
Note 1. Values of bits b7 to b1 are undefined. Only confirm the value of the RCR3.RTCEN bit.
Note 2. Skip this step when using products in which the RCR3 register is initialized by an RTC software reset.

Figure 2.3 Initialization Flowchart When Using the Sub-clock Only as a System Clock

D. When not using the sub-clock

When a crystal for the sub-clock is not connected, if the SOSCCR.SOSTP bit is 0, the MCU cannot exit software standby mode. Make sure to set both bits SOSCCR.SOSTP and RCR3.RTCEN so as to stop oscillation of the sub-clock.

Figure 2.4 shows a flowchart of the procedure described above.



Note 1. Values of bits b7 to b1 are undefined. Only confirm the value of the RCR3.RTCEN bit.

Figure 2.4 Initialization Flowchart When Not Using the Sub-clock