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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0261A/E	Rev.	1.00
Title	Notes on Self-Programming of the Flash Memory		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group, RX66N Group, RX671 Group, RX72M Group, RX72N Group	Lot No. All	Reference Document	User's Manual: Hardware for applicable products listed in the table on the last page		

This document describes a point to note on rewriting the flash memory by self-programming in the applicable products listed above.

1. Point to Note

When issuing a program command, writing of WD_{64} (in the code flash memory) or WD_2 (in the data flash memory) starts the program processing before the final value of the command, D0h, is written.
Therefore, if an interrupt occurs after WD_{64} or WD_2 has been written, the FSTATR.FRDY flag may become 1 regardless of D0h not having been written. If an FACI command is issued in the interrupt handling routine, or if a subsequent FACI command is issued using an FRDY interrupt, writing the first byte of the FACI command may cause an illegal command error.

2. Workaround

When issuing a program command (from writing of E8h to writing of D0h), disable interrupts that may trigger FACI commands.
If an interrupt occurs during the issuing of an FACI command and another FACI command is issued in the interrupt handling routine, the latter FACI command is either ignored or recognized as an illegal command, and normal operation thus cannot be expected. We recommend disabling such interrupts during the issuing of FACI commands as well as program commands.

3. Supplementary Note

When an illegal command error as described in 1. Point to Note occurs, the MCU can usually be returned to normal operation by reissuing the FACI command after general error handling. However, the MCU cannot be returned to normal operation if all of the following conditions are met. In such cases, work around the problem by the method described in 2. Workaround.

(a) A program command was issued during the suspension of erasure.
(b) An interrupt was accepted between the writing of WD_{64} or WD_2 and the writing of D0h in the above program command.
(c) An FACI command issued in the handling routine for the above interrupt.
(d) A status clear command is used to handle an illegal command error.

Note that if the first FACI command issued in the interrupt handling routine described in (c) is a P/E resume command, the first D0h byte is recognized as the final data of the program command, and an illegal command error will thus not occur, nor will resumption.

4. Reference Documents

Applicable Products	Manual Title (Document Number)
RX65N Group, RX651 Group	RX65N Group, RX651 Group User's Manual: Hardware Rev.2.30 (R01UH0590EJ0230)
RX66N Group	RX66N Group User's Manual: Hardware Rev.1.00 (R01UH0825EJ0100)
RX671 Group	RX671 Group User's Manual: Hardware Rev.1.10 (R01UH0899EJ0110)
RX72M Group	RX72M Group User's Manual: Hardware Rev.1.00 (R01UH0804EJ0100)
RX72N Group	RX72N Group User's Manual: Hardware Rev.1.00 (R01UH0824EJ0100)