RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0061A/E	Rev.	1.00
Title	Notes on Self-Programming of the Flash Memory		Information Category	Technical Notification		
Applicable Product	RA6M4 Group, RA6M5 Group, RA4M2 Group, RA4M3 Group, RA6E1 Group, RA4E1 Group, RA6T2 Group	Lot No.	Reference Document	User's Manual: Hardware for applicable products listed in the table on the last page		
		All				

This document describes a point to note on rewriting the flash memory by self-programming in the applicable products listed above.

1. Point to Note

When issuing a program command, writing of WD64 (in the user area) or WDN (in the data area) starts the program processing before the final value of the command, 0xD0, is written.

Therefore, if an interrupt occurs after WD64 or WDN has been written, the FSTATR.FRDY flag may become 1 regardless of 0xD0 not having been written. If an FACI command is issued in the interrupt handler, or if a subsequent FACI command is issued using an FRDY interrupt, writing the first byte of the FACI command may cause an illegal command error.

2. Workaround

When issuing a program command (from writing of 0xE8 to writing of 0xD0), disable interrupts that may trigger FACI commands.

If an interrupt occurs during the issuing of an FACI command and another FACI command is issued in the interrupt handler, the latter FACI command is either ignored or recognized as an illegal command, and normal operation thus cannot be expected. We recommend disabling such interrupts during the issuing of FACI commands as well as program commands.

3. Supplementary Note

When an illegal command error as described in 1. Point to Note occurs, the MCU can usually be returned to normal operation by reissuing the FACI command after general error handling. However, the MCU cannot be returned to normal operation if all of the following conditions are met. In such cases, work around the problem by the method described in 2. Workaround.

(a) A program command was issued during the suspension of erasure.
(b) An interrupt was accepted between the writing of WD64 or WDN and the writing of 0xD0 in the above program command.
(c) An FACI command issued in the handler for the above interrupt.
(d) A status clear command is used to handle an illegal command error.

Note that if the first FACI command issued in the interrupt handler described in (c) is a P/E resume command, the first 0xD0 byte is recognized as the final data of the program command, and an illegal command error will thus not occur, nor will resumption.

4. Reference Documents

Applicable Products	Manual Title
RA6M4 Group	RA6M4 Group User's Manual: Hardware Rev.1.10
RA6M5 Group	RA6M5 Group User's Manual: Hardware Rev.1.10
RA4M2 Group	RA4M2 Group User's Manual: Hardware Rev.1.10
RA4M3 Group	RA4M3 Group User's Manual: Hardware Rev.1.20
RA6E1 Group	RA6E1 Group User's Manual: Hardware Rev.1.10
RA4E1 Group	RA4E1 Group User's Manual: Hardware Rev.1.10
RA6T2 Group	RA6T2 Group User's Manual: Hardware Rev.1.20

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