To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A007A/E	Rev.	1.00
Title	Notes on R8C Family		Information Category	Technical Notification		
Applicable Products	R8C/1x Series R8C/2x Series R8C/3x Series R8C/Lx Series	Lot No. __	Reference Document			

The following notes are pertinent to the manuals listed above. Refer to individual hardware manuals to ascertain which Series have the functions shown below.

1. Note on voltage monitor interrupt and voltage monitor reset

   (This note applies to MCUs that have the voltage change detection flag.)

   When the voltage detection circuit is enabled while the voltage monitor interrupt or voltage monitor reset is disabled, low voltage is detected and the voltage change detection flag becomes 1. When low voltage is detected after the voltage detection circuit is enabled until an interrupt or a reset is enabled for the setting procedure of bits associated with voltage monitor interrupt or bits associated with voltage monitor reset, an interrupt or a reset is not generated. After an interrupt or a rest is enabled, read the voltage change detection flag. When the flag is read as 1, perform the process that occurs when low voltage is detected.

2. Note when entering wait mode by wait control bit (CM30 bit)

   (The R8C/1x Series and R8C/2x Series do not have the CM30 bit.)

   As with executing the WAIT instruction, insert at least four NOP instructions after the instruction that sets the CM30 bit to 1.

   Program example to set the CM30 bit to 1

```
BCLR 1, FMR0
BSET 0, PRCR
FCLR I
BSET 0, CM3
NOP
NOP
NOP
NOP
BCLR 0, PRCR
FSET I
```

3. Note on INTi pin

   (All INT pins apply to this note. The value for i varies according to the MCU.)

   As with changing the INT interrupt polarity select bit (INTiPL bit), when changing the INT input enable bit (INTiEN bit), the IR bit corresponding to the INTi pin may become 1 (interrupt requested). Refer to Changing Interrupt Sources in the hardware manual.

4. Note on digital filter

When the interrupt source is an input that uses a digital filter, note the following in the procedure when changing the interrupt source.

After changing the interrupt source, wait for three or more cycles of the digital filter sampling clock before setting the corresponding IR bit to 0 (no interrupt request). For more information on the instructions used to set the IR bit to 0 and related notes, refer to Rewriting Interrupt Control Register.

5. Note on timer RB

(The R8C/1x Series does not have timer RB.)

When selecting timer RA underflow as the timer RB count source, set timer RA to timer mode, pulse output mode, or event counter mode.

6. Note on timer Y

(The R8C/2x Series, R8C/3x Series, and R8C/Lx Series do not have timer Y.)

When selecting timer X underflow as the timer Y count source, set timer X to timer mode, pulse output mode, or event counter mode.

7. Notes on UARTi (i = 0 to 2)

(The value for i varies according to the MCU.)

1. When setting bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled), set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. When bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), bits FER, PER, and SUM (error flags) in the UiRB register are disabled. When read, the read value is undefined.
3. If communication is ended prematurely or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, and communication is performed again, follow the steps below:
   (1) Set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
   (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
   (3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
   (4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).
4. If communication is ended prematurely or a communication error occurs while transmitting or receiving in UART mode, and communication is performed again, follow the steps below:
   (1) Set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
   (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
   (3) Set bits SMD2 to SMD0 in the UiMR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
   (4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

8. Notes on bit operation

(This note applies to the R8C/3x Series and R8C/Lx Series.)

Set the following bits with consecutive instructions. Do not allow interrupts or DTC transfer to occur between executing instructions.

(1) PRC2 bit:

The PRC2 bit becomes 0 after setting it to 1 (write enabled) and writing to an SFR area. Write to the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts or DTC transfer between the instruction to set to the PRC2 bit to 1 and the next instruction.

(2) Bits CSPRO, FMR01, FMR02, FMR13, FMR20, FMR22, and FMR27:

When setting these bits to 1, write 0 immediately followed by 1. Do not allow interrupts and DTC transfer to occur between writing 0 and writing 1.

(3) Bits FMR14, FMR15, FMR16, and FMR17:

When setting these bits to 0, write 1 immediately followed by 0. Do not allow interrupts and DTC transfer to occur between writing 1 and writing 0.