To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A004A/E	Rev.	1.00
Title	Notes on Low-Consumption-Current Read Mode		Information Category	Technical Notification		
Applicable Products	R8C/3x Series R8C/Lx Series	Lot No.	Reference Document			

Please note the following descriptions when using low-consumption-current read mode by the FMR27 bit in the FMR register (low-consumption-current read mode enable bit).

1. Usage conditions on low-consumption-current read mode

    Low-consumption-current read mode can be used when the following conditions are met:

    - The CPU clock is divide-by-4, 8, or 16 of the low-speed on-chip oscillator clock.
    - The CPU clock is divide-by-1 (no division), 2, 4, or 8 of the XCIN clock.

    Note:

    Even if the above conditions are met, do not use low-consumption-current read mode when the CPU clock is 3 kHz or below.

2. Note when manipulating the FMR27 bit

    - After setting the CPU clock to the conditions described in number 1, set the FMR27 bit to 1 (low-consumption-current read mode enabled).
    - Set the CPU clock to conditions other than those described in number 1 when the FMR27 bit is 0 (low-consumption-current read mode disabled).
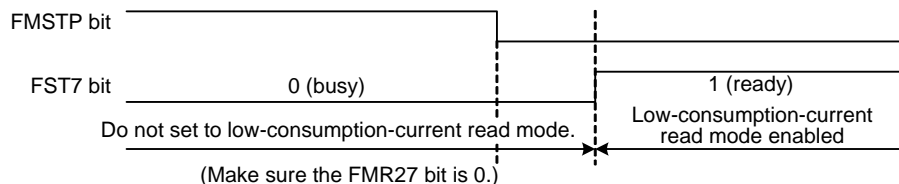
3. Note when entering wait mode or stop mode while the FMR27 bit is 1.

    Enter wait mode or stop mode after setting bits CM35 to CM37 as follows:

    - Set the CM35 bit to 0 (settings for the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register are enabled).
    - Set bits CM37 and CM36 to 00b (the MCU exits its current mode with the CPU clock immediately before entering wait mode or stop mode).

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4. Note on the FMSTP bit

    Do not set the FMR27 bit to 1 while the FMSTP bit is 1 (flash memory stops). Also, do not set the FMR27 bit to 1 when the flash memory status is busy (the FST7 bit is 0) immediately after changing the FMSTP bit from 1 to 0 (flash memory operates).

    FMSTP bit

    FST7 bit   0 (busy)   1 (ready)

            Do not set to low-consumption-current read mode.   Low-consumption-current
                                                                    read mode enabled
                    (Make sure the FMR27 bit is 0.)

5. Note on CPU rewrite mode

    Do not execute the program command, block erase command, or lock bit program command while the FMR27 bit is 1.

6. Note on the A/D converter

    Do not perform A/D conversion while the FMR27 bit is 1. Also, do not set the FMR27 bit to 1 while the ADST bit is 1 (during A/D conversion).

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