1. Notes

In the figure of “Example of Initialization Flowchart in Master Mode (SPI Operation)” in the “(8) Initialization Flowchart” of “Master Mode Operation” in “SPI Operation” of “Operation” section in the “Serial Peripheral Interface (RSPI)” chapter of the User’s Manual: Hardware of the applicable products mentioned above, when the SSLn signal (n = 0 to 3) is active high, the corresponding bit of the RSPI Slave Select Polarity Register (SSLP register) must be set to 1. In addition, when the RSPI sequence length is any value other than “1”, the sequence length must be set to the RSPI sequence control register (SPSCR).

2. Measures

With the settings mentioned above, add processing indicated with dotted lines in “Example setting of RSPI slave select polarity register (SSLP)” and “Example setting of RSPI sequence control register (SPSCR)” shown in the following page to the figure of “Example of Initialization Flowchart in Master Mode (SPI Operation).”
Example setting of the RSPI slave select polarity register (SSLP)

- Sets SSL signal polarity.

Example setting of the RSPI sequence control register (SPSCR)

- Sets SSL signal level.
- Sets RSPCK delay enable.
- Sets SSL negation delay enable.
- Sets next-access delay enable.
- Sets MSB or LSB first.
- Sets data length.
- Sets transfer bit rate.
- Sets clock phase.
- Sets clock polarity.
- Sets SSL assert signal.

Start of initialization in master mode

- Sets output mode (CMOS/Open drain).
- Sets MOSI signal value when transfer is in idle state.

Set RSPI control register 2 (SPCR2)

- Sets parity function.
- Sets interrupt mask.

Set RSPI pin control register (SPPCR)

- Sets output mode (CMOS/Open drain).
- Sets MOSI signal value when transfer is in idle state.

Set the slave select polarity register (SSLP)

- Sets SSL signal polarity.

Set RSPI command registers 0 to 7 (SPCMD0 to 7)

- Sets sequence length