To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A012A/E	Rev.	1.00
Title	Notes on Complementary PWM Mode and Reset Synchronous PWM Mode of Timer RD		Information Category	Technical Notification		
Applicable Products	See below	Lot No. __	Reference Document			

Incorrect descriptions have been found in specifications of the output level when the timer count stops during operation in timer RD complementary PWM mode and reset synchronous PWM mode for the products shown below.

1. Applicable products

R8C/20 Group, R8C/21 Group,
R8C/22 Group, R8C/23 Group,
R8C/24 Group, R8C/25 Group,
R8C/2A Group, R8C/2B Group,
R8C/2C Group, R8C/2D Group,
R8C/2K Group, R8C/2L Group,
R8C/34C Group, R8C/35A Group, R8C/35C Group,
R8C/36A Group, R8C/36C Group,
R8C/38A Group, R8C/38C Group,
R8C/3JA Group,
R8C/L3AA Group, R8C/L3AB Group, R8C/L3AC Group,
R8C/L38A Group, R8C/L38B Group, R8C/L38C Group,
R8C/L36A Group, R8C/L36B Group, R8C/L36C Group,
R8C/L35A Group, R8C/L35B Group, R8C/L35C Group,

2. Output level when timer stops

When timer RD operates in complementary PWM mode or reset synchronous PWM mode and the timer RD count stops, the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register is output from the PWM output pin.

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3. Corrections in documents

Corrections are shown in (1) to (3). (1) to (3) show changes made to tables in the Reset Synchronous PWM Mode, Complementary PWM Mode, and Notes on Timer RD sections of the Timer RD chapter.

(1) Reset synchronous PWM mode specifications

Before correction

Item	Specification
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds the output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRA0 register. The PWM output pin holds the level after the output changes by the compare match.

After correction

Item	Specification
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.) • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRA0 register. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)

(2) Complementary PWM mode specifications

Before correction

Item	Specification
Count stop condition	0 (count stops) is written to bits TSTART0 and TSTART1 in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin holds the output level before the count stops.)

After correction

Item	Specification
Count stop conditions	0 (count stops) is written to bits TSTART0 and TSTART1 when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)

(3) TRDIOji pin output level when the count stops (i = 0, 1; j = A, B, C, D)

Before correction

Stopping Count	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, write 0 to the TSTARTi bit and the count stops.	Holds the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops at compare match between registers TRDi and TRDGRAi.	Holds the output level after the output changes by the compare match.

After correction

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	The pin holds the output level immediately before the count stops. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in complementary and reset synchronous PWM modes.)
When the CSELi bit is set to 0, the count stops at compare match of registers TRDi and TRDGRAi.	The pin holds the output level after the output changes by compare match (the pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in complementary and reset synchronous PWM modes.)