Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A292A/E	Rev.	1.0
Title	Notes on Arbitration Lost in I ² C Bus Interface of the H8S/2633 Series, H8S/2643 Series and H8S/2638,2639,2630 Group		Information Category	Technical Notification		
Applicable Product	H8S/2633W Series H8S/2638W, 2639W, 2630W Group H8S/2643W Series	Lot No.		H8S/2633 Series Hardware Manual (ADE-602-165C Rev.4.0) H8S/2639, H8S/2638, H8S/2636, H8S/2630 Group Hardware Manual (REJ09B0103-0500O Rev.5.00) H8S/2643 Series Hardware Manual (ADE-602-214A Rev.2.0)		
		All	Reference Document			

Thank you for your consistent patronage of Renesas semiconductor products.

In master mode operation of the I²C bus interface, following attention is required when arbitration is lost.

1. Target Module

I²C bus interface

2. Conditions

Under the following conditions, the I²C bus interface may recognize the transmit/receive data as an address after arbitration is lost in master

mode and a transition to slave receive mode is automatically carried out.

- When a bus conflict may be occurred in multi-master mode.
- When arbitration is not lost since the address that is transmitted in the first frame is the same as the data from the other device, and output timing of the SCL matches in master mode.
- When arbitration is lost during transmission/reception of the second frame or subsequent frame, and the receive data matches the address set in the SAR or SARX register.



3. Phenomenon

The I^2C bus interface recognizes the data in transmit/receive frame as an address when arbitration is lost in master mode and a transition to slave receive mode is automatically carried out.

When arbitration is lost not in the first frame but in the second frame or subsequent frame, transmit/receive data that is not an address is compared with the value set in the SAR or SARX register as an address. If the receive data matches with the address in the SAR or SARX register, the l²C bus interface erroneously recognizes that the address call has occurred. (See figure 1.)



Figure 1 Diagram of Erroneous Operation when Arbitration is Lost

4. Restriction

In multi-master mode, a bus conflict could happen. When the I^2C bus interface is operated in master mode, check the state of the AL bit in the ICSR register every time after one frame of data has been transmitted or received.

When arbitration is lost during transmitting the second frame or subsequent frame, take avoidance measures.

5. Supplementation

Though it is prohibited in the normal I^2C protocol, the same problem may occur when the MST bit is erroneously set to 1 and a transition to master mode is occurred during data transmission or reception in slave mode.

When the MST bit is set to 1 during data transmission or reception in slave mode, the arbitration decision circuit is enabled and arbitration is lost if conditions are satisfied. In this case, the transmit/receive data which is not an address may be erroneously recognized as an address. In multi-master mode, pay attention to the setting of the MST bit when a bus conflict may occur. In this case, the MST bit in the ICCR register should be set to 1 according to the order below.

1. Make sure that the BBSY flag in the ICCR register is 0 and the bus is free before setting the MST bit.

2. Set the MST bit to 1.

3. To confirm that the bus was not entered to the busy state while the MST bit is being set, check that the BBSY flag in the ICCR register is 0 immediately after the MST bit has been set.

