To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-281A/EA	Rev.	1.0
Title	Notes on Arbitration Lost in I²C Bus Interface of the H8S Series		Information Category	Usage Limitation		
Applicable Product	H8S/2148,H8S/2138 Series H8S/2149,H8S/2169 Series H8S/2140B Series H8S/2110B H8S/2128 Series H8S/2158 Series H8S/2168 Group H8S/2194 Series H8S/2199R Series	Lot No. All	Reference Document	Following Hardware Manuals: H8S/2148 Series (ADE-602-125B Rev.3.0) H8S/2138 Series (ADE-602-144B Rev.3.0) H8S/2149, 69 Series (ADE-602-190A Rev.2.0) H8S/2140B Series (ADE-602-274A Rev.2.0) H8S/2110B (ADE-602-298 Rev.1.0) H8S/2128 Series (ADE-602-114B Rev.3.0) H8S/2158 Series (ADE-602-255A Rev.2.0) H8S/2168 Group (REJ09B0078-0300Z Rev.3.00) H8S/2194 Series (ADE-602-160A Rev.2.0) H8S/2199R Series (ADE-602-232 Rev.1.0)		

Thank you for your consistent patronage of Renesas semiconductor products.

In master mode operation of the I²C bus interface of the H8/300H Tiny Series and H8S Series, following attention is required when arbitration is lost.

1. Target Module

I²C bus interface

2. Conditions

Under the following conditions, the I²C bus interface may recognize the transmit/receive data as an address after arbitration is lost in master mode and a transition to slave receive mode is automatically carried out.

- When a bus conflict may be occurred in multi-master mode.
- When arbitration is not lost since the address that is transmitted in the first frame is the same as the data from the other device, and output timing of the SCL matches in master mode.
- When arbitration is lost during transmission/reception of the second frame or subsequent frame, and the receive data matches the address set in the SAR or SARX register.

3. Phenomenon

The I²C bus interface recognizes the data in transmit/receive frame as an address when arbitration is lost in master mode and a transition to slave receive mode is automatically carried out.

When arbitration is lost not in the first frame but in the second frame or subsequent frame, transmit/receive data that is not an address is compared with the value set in the SAR or SARX register as an address. If the receive data matches with the address in the SAR or SARX register, the I²C bus interface erroneously recognizes that the address call has occurred. (See figure 1.)

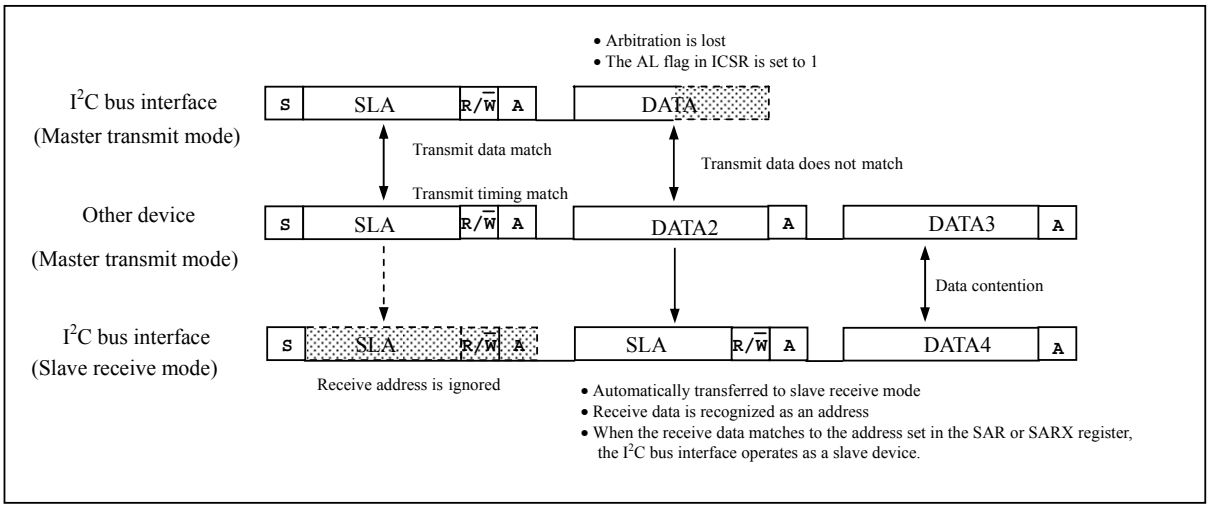

Figure 1 Diagram of Erroneous Operation when Arbitration is Lost

4. Restriction

In multi-master mode, a bus conflict could happen. When the I^{2}C bus interface is operated in master mode, check the state of the AL bit in the ICSR register every time after one frame of data has been transmitted or received.

When arbitration is lost during transmitting the second frame or subsequent frame, take avoidance measures.

5. Supplementation

Though it is prohibited in the normal I^{2}C protocol, the same problem may occur when the MST bit is erroneously set to 1 and a transition to master mode is occurred during data transmission or reception in slave mode.

When the MST bit is set to 1 during data transmission or reception in slave mode, the arbitration decision circuit is enabled and arbitration is lost if conditions are satisfied. In this case, the transmit/receive data which is not an address may be erroneously recognized as an address.

In multi-master mode, pay attention to the setting of the MST bit when a bus conflict may occur. In this case, the MST bit in the ICCR register should be set to 1 according to the order below.

1. Make sure that the BBSY flag in the ICCR register is 0 and the bus is free before setting the MST bit.
2. Set the MST bit to 1.
3. To confirm that the bus was not entered to the busy state while the MST bit is being set, check that the BBSY flag in the ICCR register is 0 immediately after the MST bit has been set.