RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A026A/E	Rev.	1.00
Title	Notes and Corrections to Manuals Regarding Port Output Enable 2 (POE) Operation in All-Module Clock Stop Mode for the RX630 Group, RX63N Group, RX631 Group, and RX63T Group		Information Category	Technical Notification		
Applicable Product	RX630 Group RX63N Group RX631 Group RX63T Group	Lot No.		RX630 Group User's Manual: Hardware Rev.1.20 (R01UH0040EJ0120)		
		All	Reference Document	RX63N Group, RX631 Group User's Manual: Hardware Rev.1.00 (R01UH0041EJ0100) RX63T Group User's Manual: Hardware Rev.1.00 (R01UH0238EJ0100)		

1. Notes and Corrections to Manuals

The POE operation is not stopped in all-module clock stop mode. High-impedance control of pins can be performed in all-module clock stop mode as well as normal operation mode.

Note that a POE interrupt request is not output and it is held inside the module in all-module clock stop mode. The interrupt request is output after exiting all-module clock stop mode.

2. Details on Corrections

The corrections are indicated in red in the list below.

[RX630, RX63N, RX631]

Description in 11.6.2.1 Transition to All-Module Clock Stop Mode is corrected as follows:

"executing a WAIT instruction while the SBYCR.SSBY bit is 0 stops the bus controller, I/O ports, and all modules except for the 8-bit timers, POE, IWDT, RTC, power-on reset circuit, voltage detection circuit at the end of the current bus cycle, and the chip enters all-module clock stop mode"

[RX63T]

Description in 11.5.2.1 Transition to All-Module Clock Stop Mode is corrected as follows:

"executing a WAIT instruction while the SBYCR.SSBY bit is 0 stops the bus controller, I/O ports, and all modules except for POE, the IWDT, power-on reset circuit, voltage detection circuit at the end of the current bus cycle, and the chip enters all-module clock stop mode."

