1. Notes and Corrections to Manuals

The POE operation is not stopped in all-module clock stop mode. High-impedance control of pins can be performed in all-module clock stop mode as well as normal operation mode. Note that a POE interrupt request is not output and it is held inside the module in all-module clock stop mode. The interrupt request is output after exiting all-module clock stop mode.

2. Details on Corrections

Description in 11.6.2.1 Transition to All-Module Clock Stop Mode is corrected as follows (the change is indicated in red):
"executing a WAIT instruction while the SBYCR.SSBY bit is 0 stops the bus controller, I/O ports, and all modules except for the 8-bit timers, POE, IWDT, RTC, power-on reset circuit, voltage detection circuit at the end of the current bus cycle, and the chip enters all-module clock stop mode"