To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A693A/E	Rev.	1.00
Title	Notes about using Deep Standby Mode of SH7263/SH7203		Information Category	Technical Notification		
Applicable Product	SH7263 Group SH7203 Group	Lot No. ALL	Reference Document	SH7263 Group Hardware Manual (REJ09B0290-0200) SH7203 Group Hardware Manual (REJ09B0313-0200)		

We would like to inform you of addition of notes about canceling deep standby mode by an interrupt in hardware manual of applicable products.

Before change

Section 32 (SH7263) / 28 (SH7203) Power-Down Modes

32.3.4 (SH7263) / 28.3.4 (SH7203) Deep Standby Mode

(2) Canceling Deep Standby Mode

・Canceling by an interrupt

When the falling edge or rising edge of the NMI pin (selected by the NMI edge select bit (NMIE) in interrupt control register 0 (ICR0) of the interrupt controller (INTC)) or the falling edge or rising edge of an IRQ pin (IRQ7 to IRQ0 assigned to PE11 to PE4) (selected by the IRQn sense select bits (IRQn1S and IRQn0S) in interrupt control register 1 (ICR1) of the interrupt controller (INTC)) is detected, clock oscillation is started after the wait time for the oscillation settling time. After the oscillation settling time has elapsed, deep standby mode is cancelled and the power-on reset exception handling is executed.

The clock output phase of the CKIO pin may be unstable immediately after detecting an interrupt and until deep standby mode is canceled. When deep standby mode is canceled by the falling edge of the NMI pin, the NMI pin should be high when the CPU enters deep standby mode (when the clock pulse stops) and should be low when deep standby mode is canceled (when the clock is initiated after oscillation settling). When deep standby mode is canceled by the rising edge of the NMI pin, the NMI pin should be low when the CPU enters deep standby mode (when the clock pulse stops) and should be high when deep standby mode is canceled (when the clock is initiated after oscillation settling). (The same applies to the IRQ pin.)

After change (addition of red letters)

Section 32 (SH7263) / 28 (SH7203) Power-Down Modes

32.3.4 (SH7263) / 28.3.4 (SH7203) Deep Standby Mode

(2) Canceling Deep Standby Mode

・Canceling by an interrupt

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The clock output phase of the CKIO pin may be unstable immediately after detecting an interrupt and until deep standby mode is canceled. When deep standby mode is canceled by the falling edge of the NMI pin, the NMI pin should be high when the CPU enters deep standby mode (when the clock pulse stops) and should be low when deep standby mode is canceled (when the clock is initiated after oscillation settling). When deep standby mode is canceled by the rising edge of the NMI pin, the NMI pin should be low when the CPU enters deep standby mode (when the clock pulse stops) and should be high when deep standby mode is canceled (when the clock is initiated after oscillation settling). (The same applies to the IRQ pin.)

Also, about NMI and the all interrupt pins (IRQ) which are selected by DSSSR to cancel deep standby mode, regardless whether they will really cancel deep standby mode or not,

(1) For the pins which are set as rising edge, those should be low when the CPU enters deep standby mode

(2) For the pins which are set as falling edge, those should be high when the CPU enters deep standby mode