Date: Dec. 14, 2017

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A043A/E	Rev.	1.00
Title	Notes about SSCG		Information Category	Technical Notification		
Applicable Product	See following	Lot No. All	Reference Document	See following		

In the products listed in bellow, a bug about SSCG function is found. There is a possibility that SSCG function can not modulate clock frequency properly.

The details is shown in below.

Applicable products and relevant documents

Applicable products		Relevant documents	Rev.	Document number
series	Group			
RZ/A	RZ/A1H, RZ/A1M	RZ/A1H Group, RZ/A1M Group User's Manual: Hardware	Rev 3.00	R01UH0403EJ0300
	RZ/A1L, RZ/A1LU, RZ/A1LC	RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group User's Manual: Hardware	Rev 3.00	R01UH0437EJ0300

[1] Condition

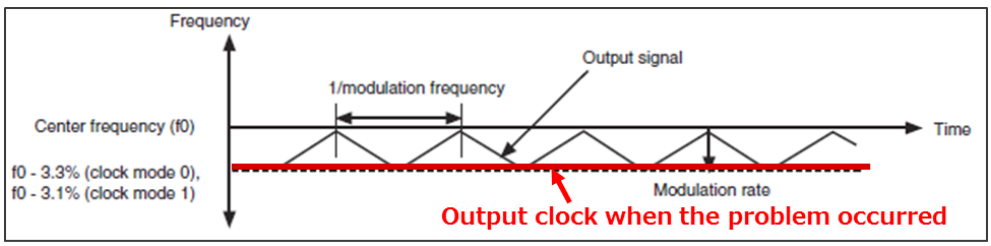
When SSCG is used and fulfill more than one of following conditions.

- The power is supplied in the power on sequence as following order
  1) Supply 3.3 volt power and MD_CLKS pin is changed to high level (SSCG ON)
  2) Supply 1.2 volt power
- Deep standby mode is cancelled by power on reset and MD_CLKS pin is asserted high level during power on reset period.
- Deep standby mode is cancelled by other than power on reset.

Detail condition is described in "[4] Detail Condition".

[2] Phenomenon

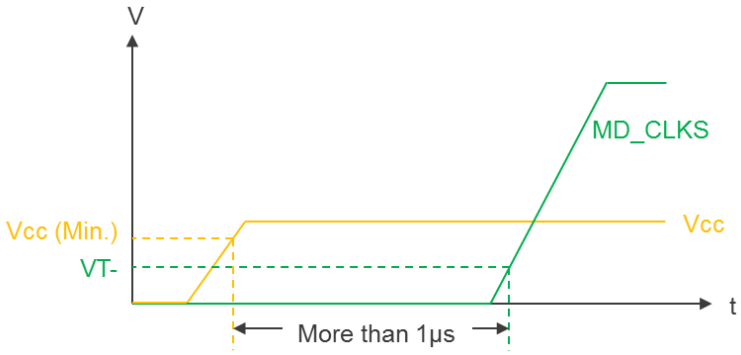
There is a possibility that clock modulation function does not work and the frequency is fixed to the lower limit frequency.



[3] Workaround

There is no software workarounds. Please apply the following hardware workarounds.

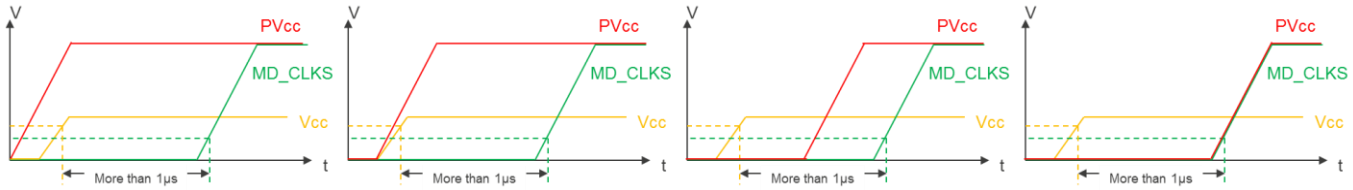
- Please make more than one microsecond between Vcc power on and change timing of MD_CLKS pin to high level. (below figure)
  And do not use deep standby mode.



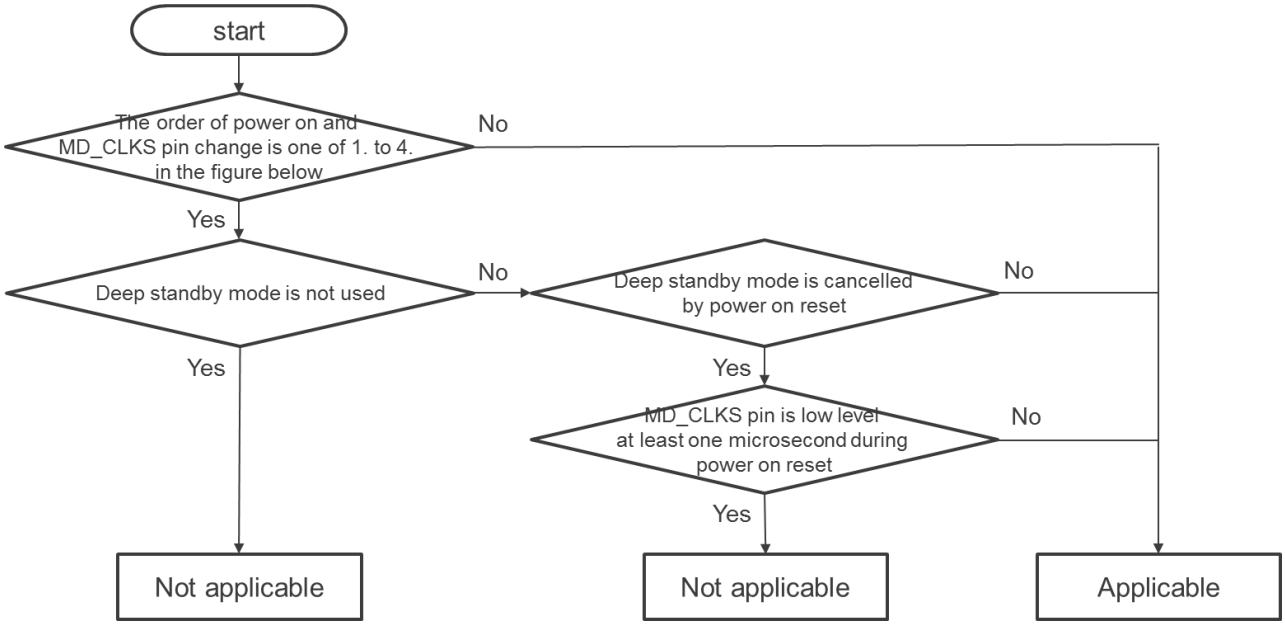
From Electrical Characteristics (DC) in
- RZ/A1H Group, RZ/A1M Group
  User's Manual: Hardware
- RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group
  User's Manual: Hardware

Vcc (Min.) = 1.10V
VT- = 0.8V

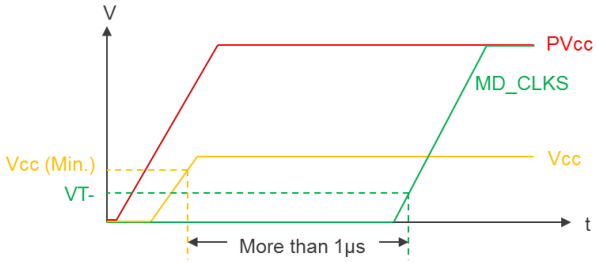
- PVcc power on timing should be at the same time as MD_CLKS pin or faster than MD_CLKS pin. (below figure)
  if PVcc power on timing is later than change timing of MD_CLKS pin to high level, it becomes absolute maximum rating violation.



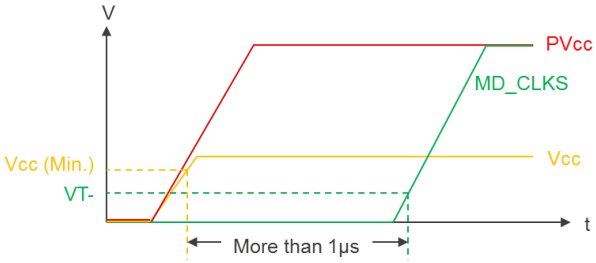
[4] Detail Condition



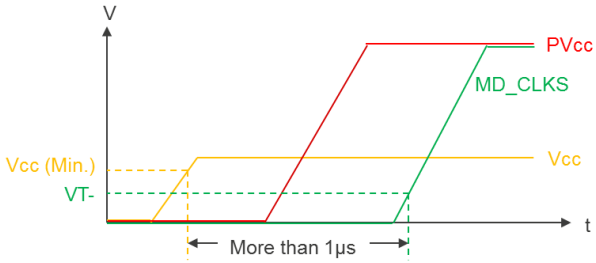
1. In case of order of PVcc, Vcc, MD_CLKS



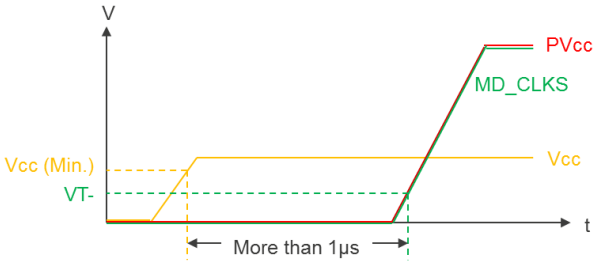
2. In case of order of PVcc = Vcc, MD_CLKS



3. In case of order of Vcc, PVcc, MD_CLKS



4. In case of order of Vcc, PVcc = MD_CLKS



From Electrical Characteristics (DC) in
- RZ/A1H Group, RZ/A1M Group
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End of document