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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A853A/E	Rev.	1.00
Title	Notes about panel clock generation of Video Display Controller 4		Information Category	Technical Notification		
Applicable Product	SH7268 Group SH7269 Group	Lot No. All	Reference Document	SH7268 Group, SH7269 Group User'sManual: Hardware Rev1.00 (R01UH0048EJ0100)		

We would like to inform you of the notice about panel clock generation of Video Display Controller 4.

【Notice】

(1) When input clock from VIDEO_X1 when releasing power-on reset or returning to deep standby mode and selecting 1/7 frequency division, panel clock may not operate normal output.

※When VIDEO_X1 is fixed to "Low" or "High", panel clock operate normal output.

(2) When changing the input source of the panel clock by means of the PANEL_ICKSEL[1:0] bit in SYSCNT_PANEL_CLK or the INP_SEL bit in INP_SEL_CNT and selecting 1/1,1/2,1/5,1/9 frequency division, panel clock may not operate normal output.

【Workaround】

(1) Specifying 1/7 frequency division

In the initial settings after a power-on reset or deep standby mode and when changing the input source of the panel clock by means of the INP_SEL bit in the INP_SEL_CNT and the PANEL_ICKSEL [1:0] bits in the SYSCNT_PANEL_CLK, do not fail to perform the steps below to confirm that the 1/7 clock ratio output is selected for the panel clock.

(a) After specifying the panel clock input source by means of the INP_SEL bit in the INP_SEL_CNT and the PANEL_ICKSEL [1:0] bits in the SYSCNT_PANEL_CLK, set the PANEL_DCDR[5:0] bits in the SYSCNT_PANEL_CLK to specify 1/7 as the clock ratio.

(b) Set the PANEL_ICKEN bit in the SYSCNT_PANEL_CLK to 1.

(c) In the scaling block, set the period of the vertical sync signal.

(d) Set to 1 the TCON_VEN bit in the TCON_UPDATE.

(e) After the vertical sync signal period set in (d) has elapsed, read the TCON_VEN bit in the TCON_UPDATE.

If the read value is 0, the panel clock is being output correctly and the setting procedure is complete.

If the read value is 1, the panel clock output is fixed at low or high level.

(f) If the output is fixed, initialize video display controller 4 by means of the VDC4SRST bit in the SWRSTCR2 of the power-down modes, then redo the setting procedure from (a).

(2) Specifying 1/3, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, or 1/32 frequency division

In the initial settings after a power-on reset or deep standby mode and when changing the input source of the panel clock by means of the INP_SEL bit in the INP_SEL_CNT and the PANEL_ICKSEL[1:0] bits in the SYSCNT_PANEL_CLK, do not fail to perform the steps below to confirm that the 1/12 clock ratio output is selected for the panel clock, then specify the desired clock ratio. If the 1/12 clock ratio output is abnormal, output at the desired clock ratio will also be abnormal.

(a) After specifying the panel clock input source by means of the INP_SEL bit in the INP_SEL_CNT and the PANEL_ICKSEL[1:0] bits in the SYSCNT_PANEL_CLK, set the PANEL_DCDR[5:0] bits in the SYSCNT_PANEL_CLK to specify 1/12 as the clock ratio.

(b) Set the PANEL_ICKEN bit in the SYSCNT_PANEL_CLK to 1.

(c) In the scaling block, set the period of the vertical sync signal.

(d) Set to 1 the TCON_VEN bit in the TCON_UPDATE.

(e) After the vertical sync signal period set in (d) has elapsed, read the TCON_VEN bit in the TCON_UPDATE.

If the read value is 0, set the PANEL_DCDR[5:0] bits in the SYSCNT_PANEL_CLK to specify the desired clock ratio and complete the setting procedure.

If the read value is 1, the panel clock output is fixed at low or high level.

(f) If the output is fixed, initialize video display controller 4 by means of the VDC4SRST bit in the SWRSTCR2 of the power-down modes, then redo the setting procedure from (a).

(3) Specifying a frequency division ratio other than the above

There is no need to confirm the division ratio of the panel clock output.

(a) After specifying the panel clock input source by means of the INP_SEL bit in the INP_SEL_CNT and the PANEL_ICKSEL[1:0] bits in the SYSCNT_PANEL_CLK, set the PANEL_DCDR[5:0] bits in the SYSCNT_PANEL_CLK to specify the desired clock ratio.

(b) Set the PANEL_ICKEN in the SYSCNT_PANEL_CLK to 1.