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On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A663A/E	Rev.	1.00
Title	Note on use of SH7780 PCIC Host Bus Bridge Mode and Manual Correction		Information Category	Technical Notification		
Applicable Product	SH7780 Group	Lot No. All lots	Reference Document	SH7780 Hardware Manual Rev.1.00 Dec.13.2005 (REJ09B0158-0100)		

There is a usage note about the PCIC of the SH7780.

If using the PCIC in host bus bridge mode (MODE6: low level) with the following condition (1) to (4) all, use the workaround shown below. Regarding this information, there are some manual corrections.

1. Note on use of SH7780 PCIC host bus ridge mode

[Summary]

When using the PCIC in host bus bridge mode with the following condition (1) to (4) all, the PCI bus request from the device of lower priority REQn# (#: low active) than REQm# (n>m) may be masked in the PCIC, and the PCI bus arbitration may not be performed correctly. And even if the lower priority device keeps asserting its REQn#, the corresponding GNTn# is not asserted, as the result, the transfer request of the REQn# device is not executed and then the master broken error of the REQn# device (PCIAINT.MBI=1) and the REQn# error (PCIBMIR.REQnBME=1) may occur.

[Condition]

(1) Selecting the PCI bus arbitration mode is fixed mode (PCICR.BMAM=0).

(2) There are two or more external PCI devices except the SH7780 that may become a master.

(3) There is at least one device that does not negate the REQ# on the same clock timing of the FRAME# assertion (the REQ# negation is one or more clock later than the FRAME# assertion *1) when a transaction (single and burst transfer) is executed. (REQm# in the following figure)

(4) There is an external PCI device that may become a master and has the lower priority (REQn#) than the above device (REQm#).

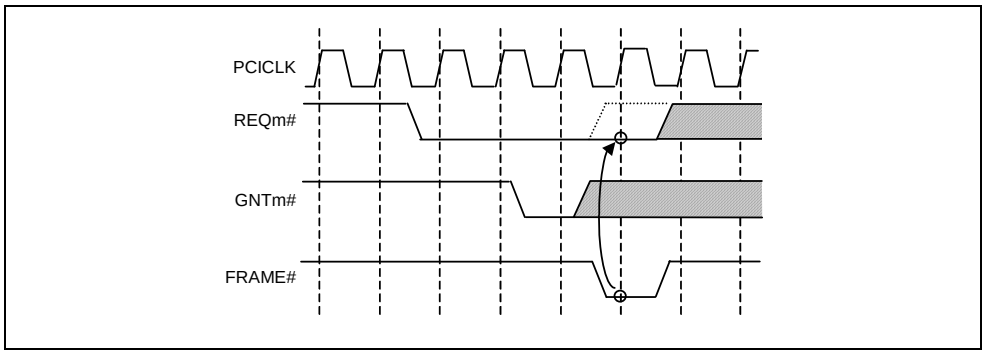


Figure. Example of REQ# Negation and FRAME# Assertion are not Same Clock Timing

Note *1: It is not included that the REQ# is asserted continuously for a next transaction.

[Workaround]

An external PCI device that does not negate the REQ# on the same clock timing of the FRAME# assertion (REQm# in above figure) may become a master; use the following workaround either (1) or (2).

(1) Use pseudo round robin mode for arbitration.

Select pseudo round robin mode for the PCI bus arbitration (PCICR.BMAM-1). When using round robin mode, the REQn# is not masked in the PCIC and the PCI bus arbitration is performed correctly.

(2) The priority of the corresponding timing device (REQm# in above figure) is made the lowest priority.

In case of only one device that does not negate the REQ# on the same clock timing of the FRAME# assertion, made the priority level of the corresponding device to lowest (connect the corresponding device to the lowest REQn# and GNTn#).

2. Manual correction

In relation to above content, there are following manual correction.

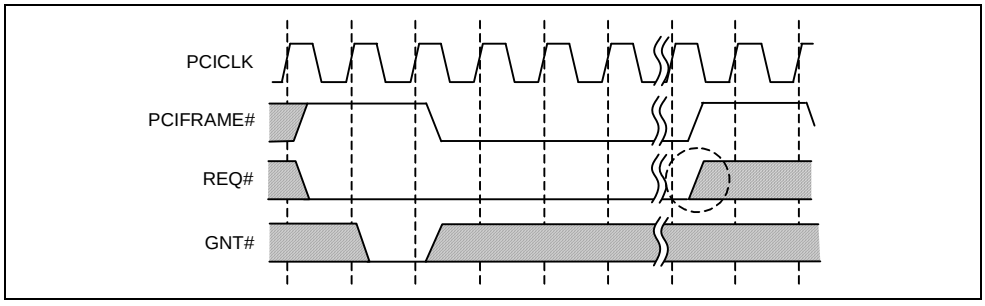
[Correction]

SH7780 PCIC normal mode REQ# negation timing are corrected as follows.

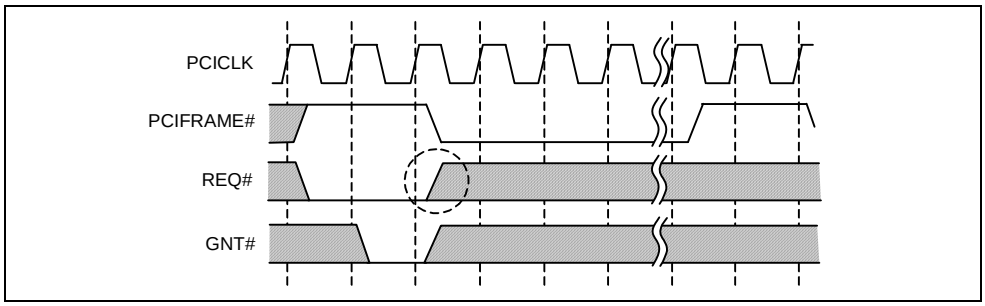
Figure 13.19 and 13.20 REQ# negation timing are corrected as follows.

For details, refer to SH7780 hardware manual (REJ09B0158-0100) p548 “Figure 13.19 Master Write Cycle in Normal Mode (Burst)”, and p549 “Figure 13.20 Master Read Cycle in Normal Mode (Burst)”.

Before correction



After correction



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