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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0212A/E	Rev.	1.00
Title	Note on Software Reset of the DMA Controller for the Ethernet Controller (EDMAC) of RX64M and RX71M Group Products		Information Category	Technical Notification		
Applicable Product	RX64M Group RX71M Group	Lot No. All	Reference Document	RX64M Group User's Manual: Hardware Rev.1.10 (R01UH0377EJ0110) RX71M Group User's Manual: Hardware Rev.1.10 (R01UH0493EJ0110)		

This document is a cautionary note regarding software reset of the DMA controller for the Ethernet controller (EDMAC) in products of the RX64M and RX71M Groups.

1. Note

When the corresponding EDMR.SWR bit is set to 1 while data transfer by the EDMAC0, EDMAC1, or PTPEDMAC is in progress, data in the address range from 0000 0000h to 0000 001Fh may be destroyed.

2. Countermeasures

A. When addresses from 0000 0000h to 0000 001Fh are not in use (or when the destruction of data in this address range will not create a problem)

Apply a software reset according to the procedure described in section 35.5.3, Handling Errors in Control Information, of the user's manual.

(1) Write 0000 0001h (reset EPTPC) to the EPTPC.PTRSTR register.
(2) Write 0000 0001h (reset PTPEDMAC) to the PTPEDMAC.EDMR register.
(3) Write 0000 0001h (reset ETHERCn and EDMACn) to the EDMACn.EDMR registers of the two channels.
(4) Wait for 64 cycles of the PCLKA to allow initialization to be completed.
(5) Write 0000 0000h (release reset of EPTPC) to the EPTPC.PTRSTR register.
(6) Wait for 256 cycles of the PCLKA until the EPTPC is released from the reset.

B. When addresses from 0000 0000h to 0000 001Fh are in use

Apply a software reset after stopping communications according to the procedure below.

(1) Set the ETHERCn.ECMR.RE bit to 0 (disable receive function).

(2) Wait for completion of the write-back to the receive descriptor.

(3) Confirm that the EDTRR.TR bits in the EDMACn and PTPEDMAC have become 0 (transmission is completed).

(4) Write 0000 0001h (reset EPTPC) to the EPTPC.PTRSTR register.

(5) Write 0000 0001h (reset PTPEDMAC) to the PTPEDMAC.EDMR register.

(6) Write 0000 0001h (reset ETHERCn and EDMACn) to the EDMACn.EDMR registers of the two channels.

(7) Wait for 64 cycles of the PCLKA to allow initialization to be completed.

(8) Write 0000 0000h (release reset of EPTPC) to the EPTPC.PTRSTR register.

(9) Wait for 256 cycles of the PCLKA until the EPTPC is released from the reset.